Meeting the 5 Key DDR5 Test Challenges as We Migrate to Next Gen Memory

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Meeting the 5 Key DDR5 Test Challenges as We Migrate to Next Gen Memory Webinar

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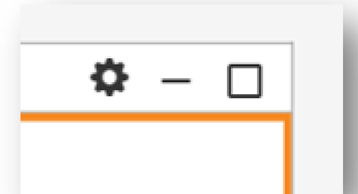
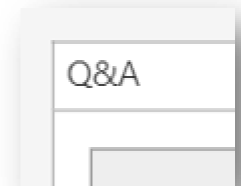
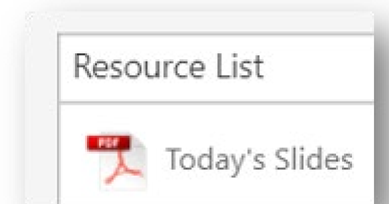






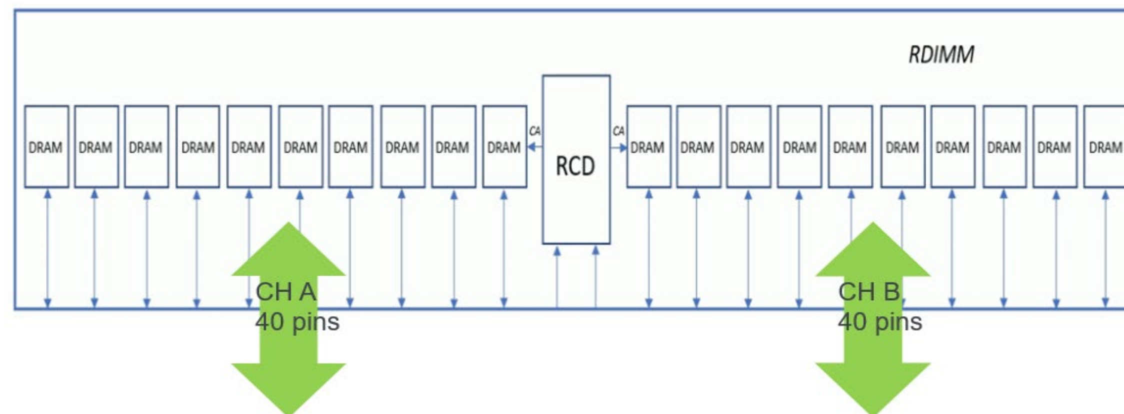
DDR5 – What's NEW

- Higher Data Rate -> Current: 3200 to 6400 Mbps
- Higher Density -> 8Gb – 64Gb monolithic dies
- Lower voltage -> 1.1V, Internal DQ/CA VREF
- DQS-DQ offset -> Writes are not center aligned
- Reads can have an offset as well
- Reduced CA pin count. No RAS/CAS/WE
- Dynamic ODT

- DRAM Rx equalization -> 4 tap DFE
- Standalone DRAM Tx/Rx characterization
- Dedicated DQS/DQ Rx Loopback pins

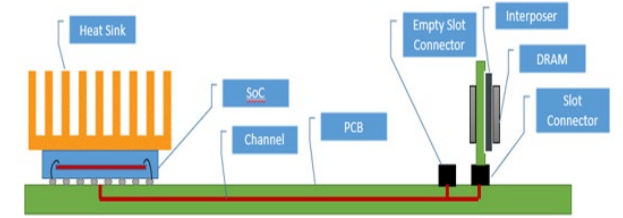
- Duty Cycle Adjuster (DCA)
- DQS Interval Oscillator Circuit
- New Training Modes
  - New Read Preamble Training
  - CS Training
  - Command Address Training (CBT)
  - Write Levelling
  - DQS Oscillator training
- Internal Reference Voltage for DQ/CA

- Two independent 40 bit (32-bit + ECC) channels
- Higher Burst Length
- Higher prefetch
- Increased Bank Groups
- Single Error Correction ECC



DDR5 Rev1.0 spec released in July 2020. To access the spec, please visit JEDEC

DDR5 SI Validation Overview



System Level Tx (In-System Test)

- High Performance Scope
- High Impedance Probes
- SI Interposers

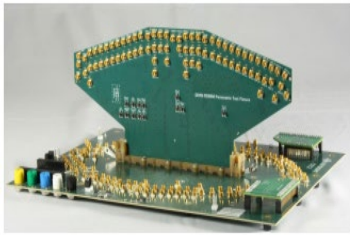
JEDEC Electrical & Timing Parameters
- Clock Jitter, DQ/CA Eye
- CA, Write & Read timing
- VIX, VIHL, OV/US etc

NEW

DRAM TX Conformance

- High Performance Scope
- CTC and PTF Boards
- SMA Cables
- TDR

- Tx DQ/DQS Jitter
- Tx DQ Stressed Eye



NEW

DRAM RX Conformance

- BERT/Pattern Generator
- High Performance Scope
- CTC and PTF Boards
- SMA Cables

- DQS Jitter Sensitivity
- DQ/DQS Voltage Sensitivity
- Rx DQ Stressed Eye

Memory Validation Challenges

DDR5 System Tx Test Challenges

4-TAP RX DFE

SIGNAL ACCESS

BURST SEPARATION

PROBE LOADING

DE-EMBEDDING

DEBUG

Memory Validation Challenges

DE-EMBEDDING

Challenge:

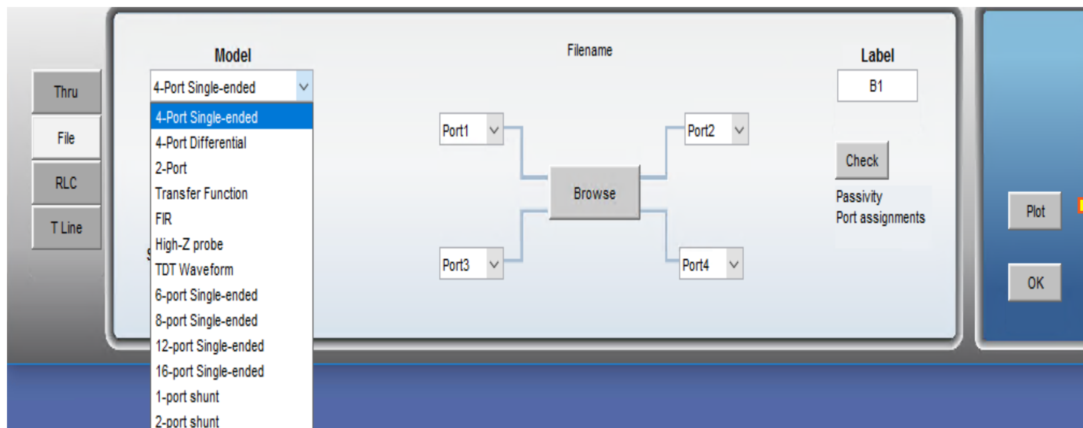
- Mid-bus probing causes reflections
- Interposer and probes loads the bus
- Probe close the the Rx and not DRAM ball
- Need s-par files from multiple sources - SOC, Boards, DRAM, Interposer, Probe etc
- Garbage In, Garbage Out

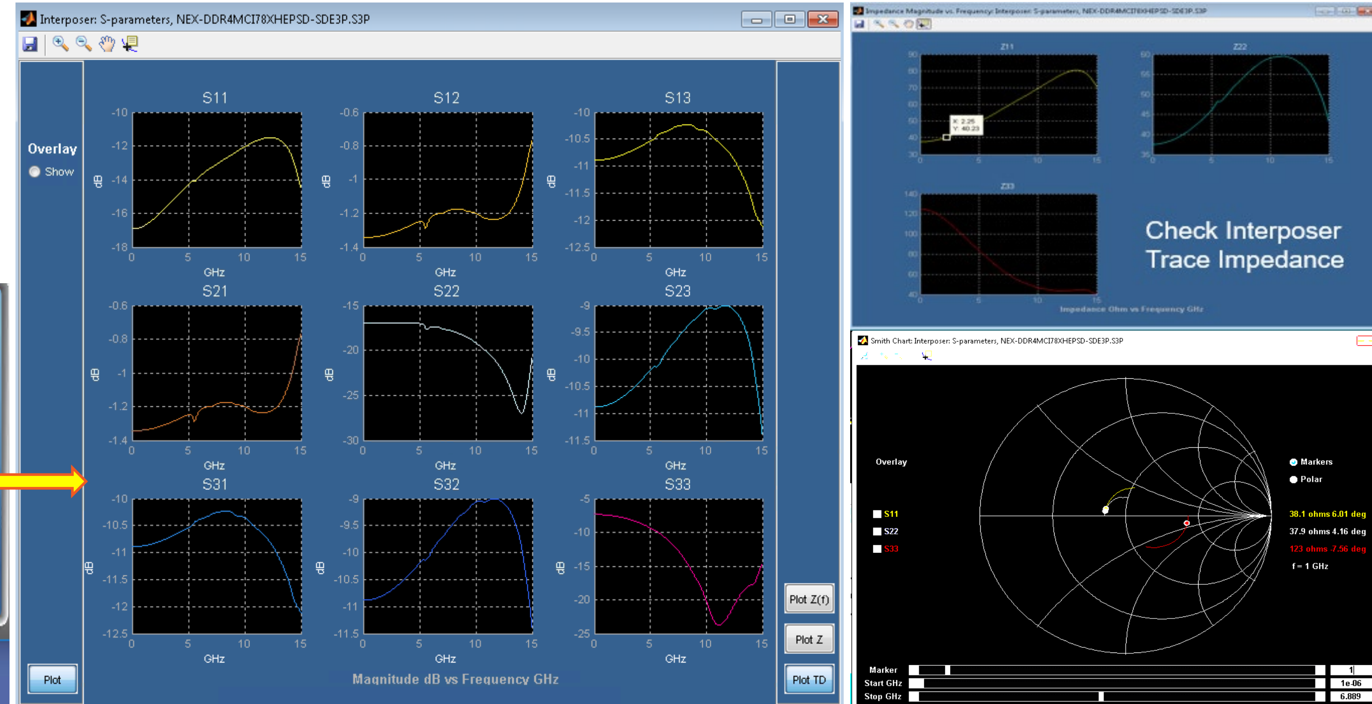
Solution: SDLA (Serial Data Link Analysis) Scope SW

- Validate the quality of s-par files upfront
- Remove the effect of probe and interposers
- **Virtual Probing** - Allows the user to move the probe point from the DRAM ball to the memory die.
- Perform What-If analysis.

How to check the quality of s-par files?

- Resample non-uniform s-par file
- Check Passivity and Port Assignments
- Plot S-parameters and Smith Charts



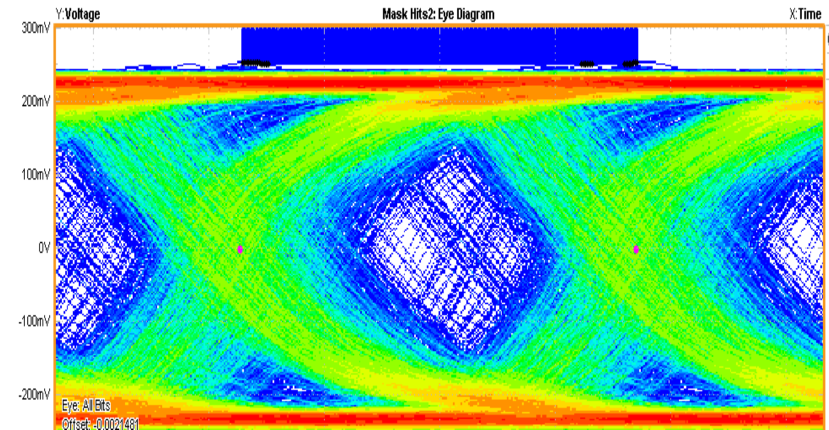


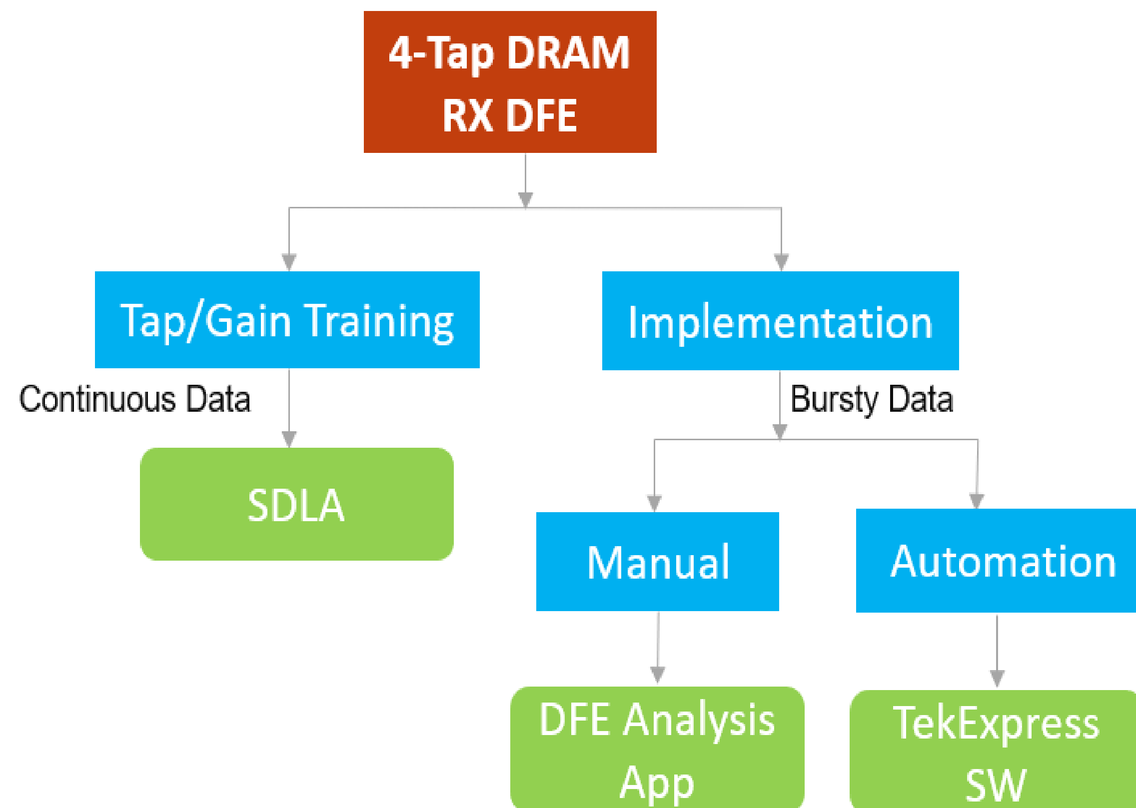
Memory Validation Challenges

RX DFE ON BURSTY DDR SIGNALS

Challenge:

- Data eye is expected to be closed at a DRAM ball at higher speeds. User will need to apply DFE to open up the data eye.
- How do I train the DFE taps?
- How do I apply DFE on bursty DDR traffic?
- How do I characterize DFE?
- How do I debug at a system level with DFE?





Solution:

- **SDLA - Train the DFE Tap and Gain values**
- **TekExpress – Automation Compliance SW**
- **DFE Analysis App – Debug/Manual Operation**

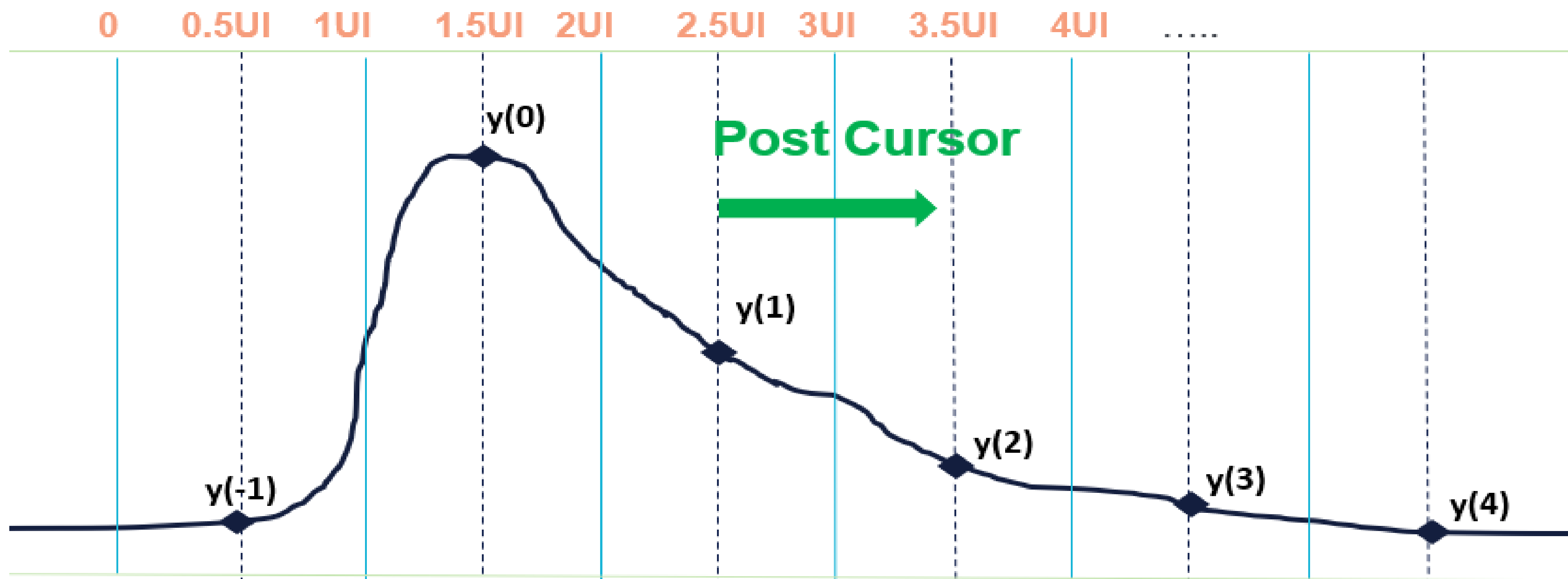
DFE Tap Value

MANUAL CALCULATION

I don't know the DFE Tap values. Where do I start?

1. Product/System level simulations
2. DRAM mode registers

DFE tap value can be easily calculated manually using a single high pulse ISI pattern

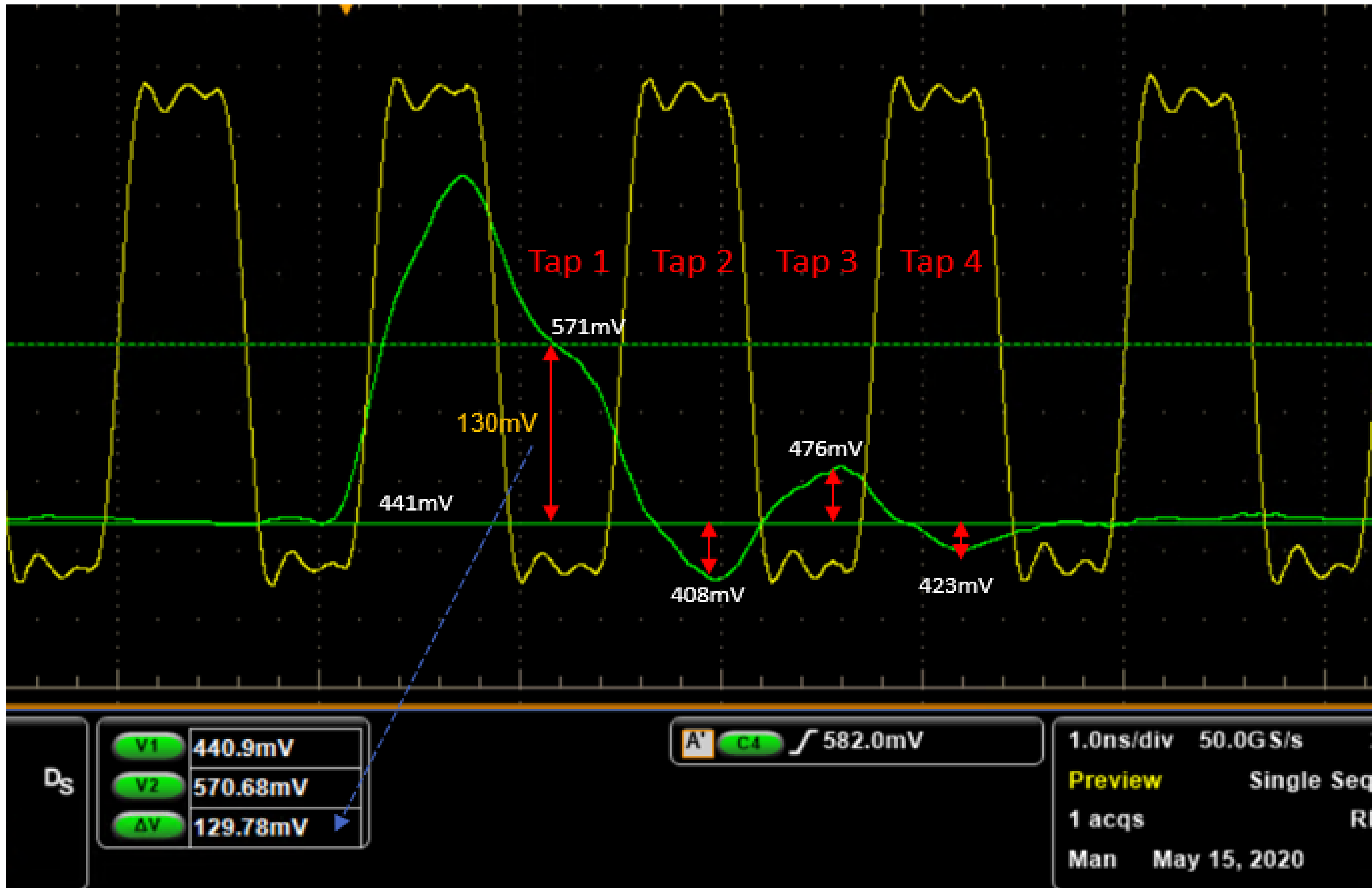


Tap Values:

- b1 = - (y(1) - y(-1)) / 2
- b2 = - (y(2) - y(-1)) / 2
- b3 = - (y(3) - y(-1)) / 2
- b4 = - (y(4) - y(-1)) / 2

DFE Tap Calculation

SCOPE WAVEFORMS



Tap1 = -(571-441)/2 = -65 mV

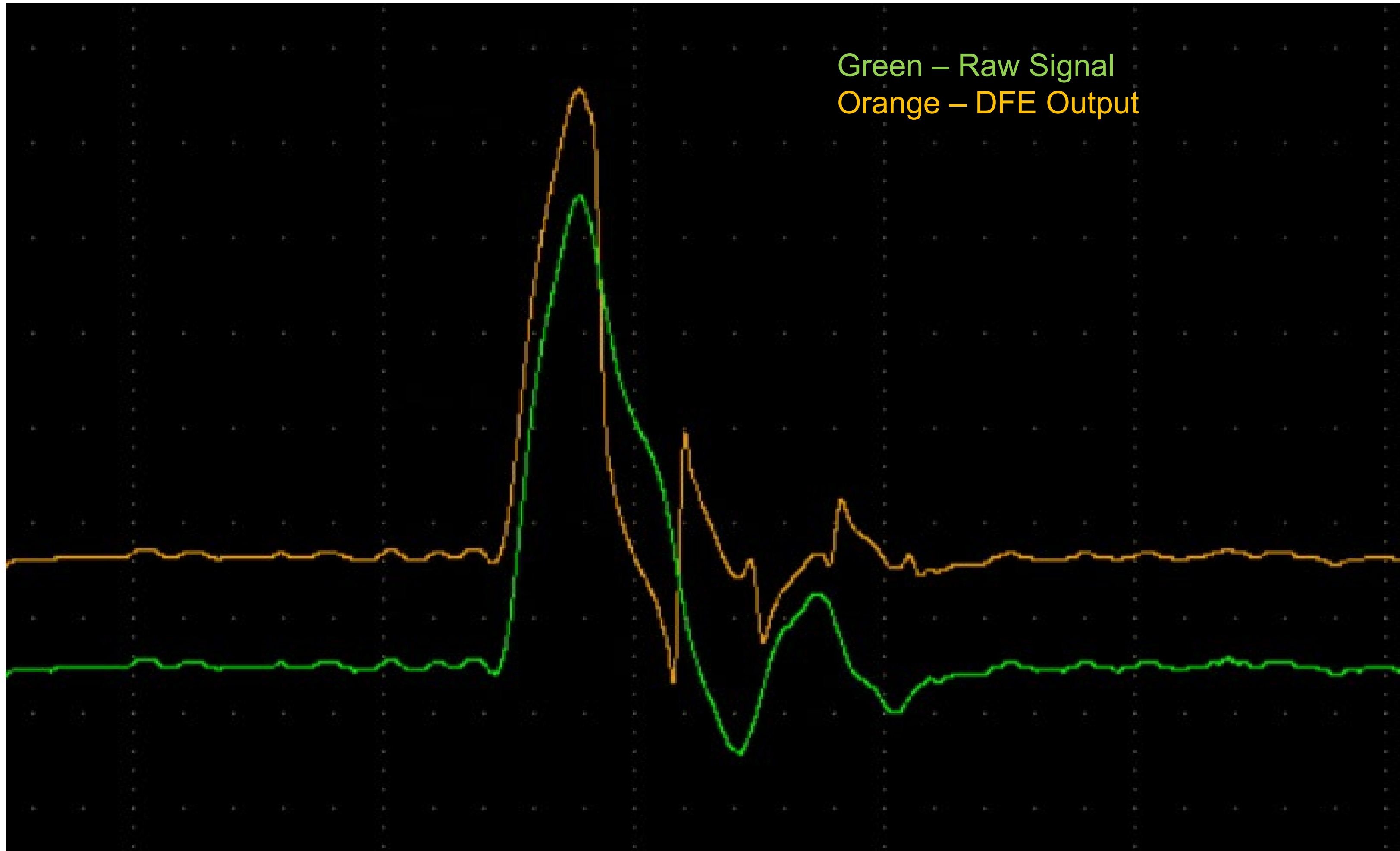
Tap2 = - (408 – 441)/2 = +17mV

Tap3 = - (476-441)/2 = -18mV

Tap4 = - (423-441)/2 = +9mV

DFE Scope Output

PRE/POST DFE OUTPUT COMPARISON



Gain	Tap1
0dB	-65mV
Threshold	Tap2
580mV	17mV
	Tap3
	-18mV
	Tap4
	9mV

Memory Validation Challenges

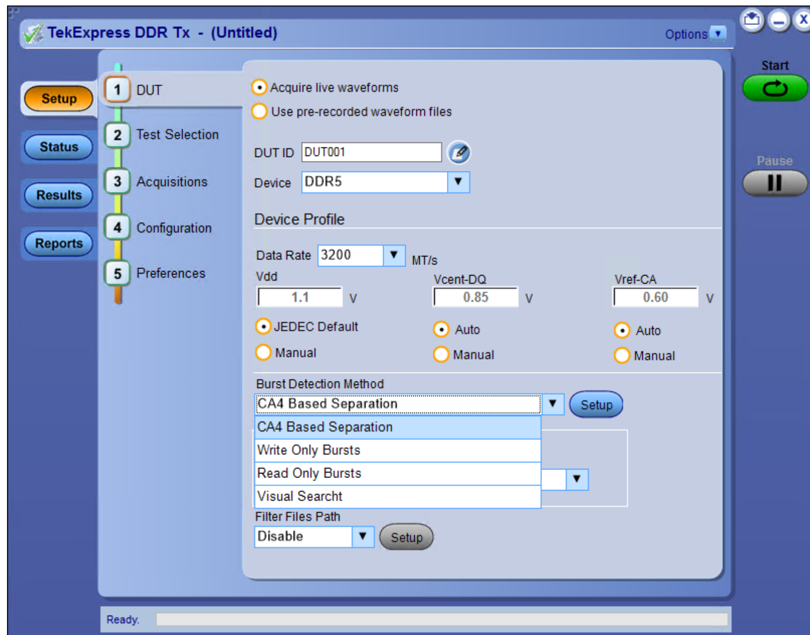
READ/WRITE BURST DETECTION & SEPARATION

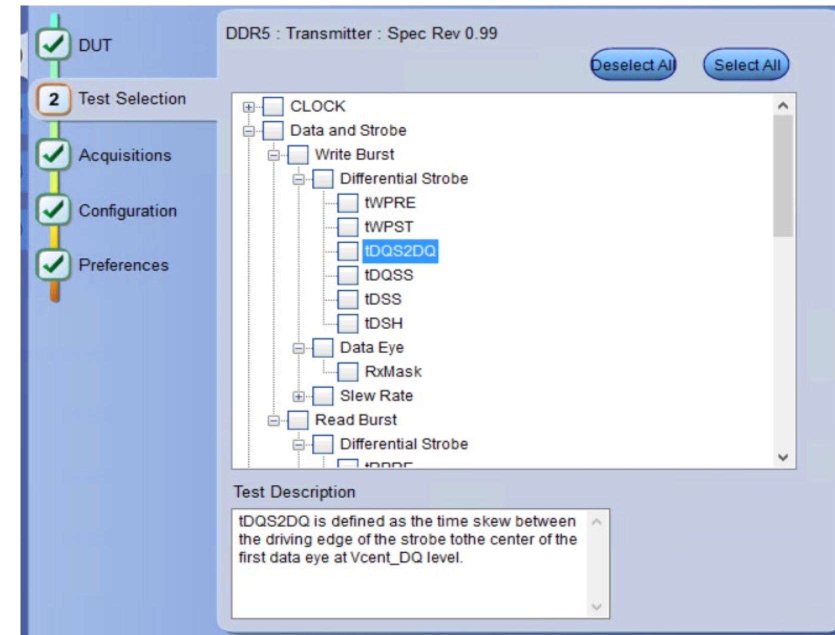
Challenge:

- DQS-DQ is not center aligned for writes. How do I measure this delay - tDQS2DQ?
- Reads can also have an offset up to 3UI
- Similar Preamble and Postamble for Read & Write bursts.

Solution: New Algorithms in TekExpress Scope SW

- Burst detection based on Amplitude, Burst Length and pre and post-ambles.
- Auto measurement of write tDQS2DQ (DQS-DQ offset) for improved burst separation.





DRAM RX OVERVIEW

Tektronix

DDR5 Rx Test Challenges

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Introduction to DDR5 Rx Testing

WHAT NEEDS TO BE TESTED?

- One-word answer – RECEIVERS
- How do we test a DDR digital receiver?
  - Signal Amplitude Sensitivity -- DQ (data) or DQS (clock)
  - Clock Jitter Sensitivity
  - Stressed-Eye Sensitivity
- Both “Conformance-Only” and “Deep-Dive” measurements

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Where Are the DDR5 Receivers?

EVERYWHERE….

- DDR5 Receivers are found in many of the individual component IC's used in DDR5 Applications
  - DRAMs
  - RCD (Register Clocking Devices)
  - DB (Data Buffers)
  - ASIC Memory Controllers
- These receivers have to operate over temperature from 3.2-6.4 Gbps
  - With stretch goals to get up to 8.4Gbps (that's 312 to 119 psec/bit)

Receiver Testing Is New to DDR Memory

WHY NOW?

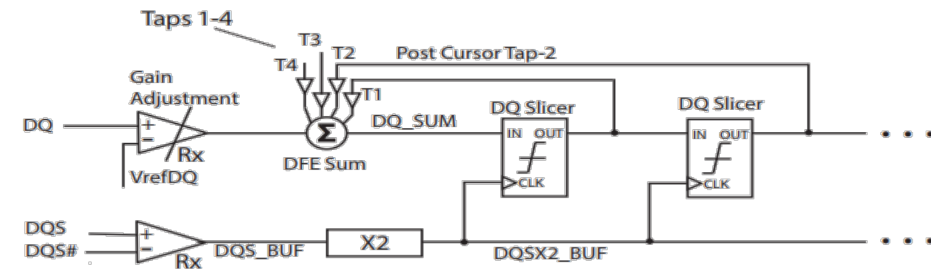
- High-Speed
  - Up to 8.4 Gbps
- Increased Crosstalk
  - Faster data rates means faster edges and faster edges induce more crosstalk
- Increased Reflections
  - Reflections from multi-terminated DDR applications increase with higher frequencies
- Along with other changes, DDR5 now employs **Decision Feedback Equalization** (DFE)
  - DFE improves eye openings in face of Inter-Symbol Interference (ISI) and crosstalk

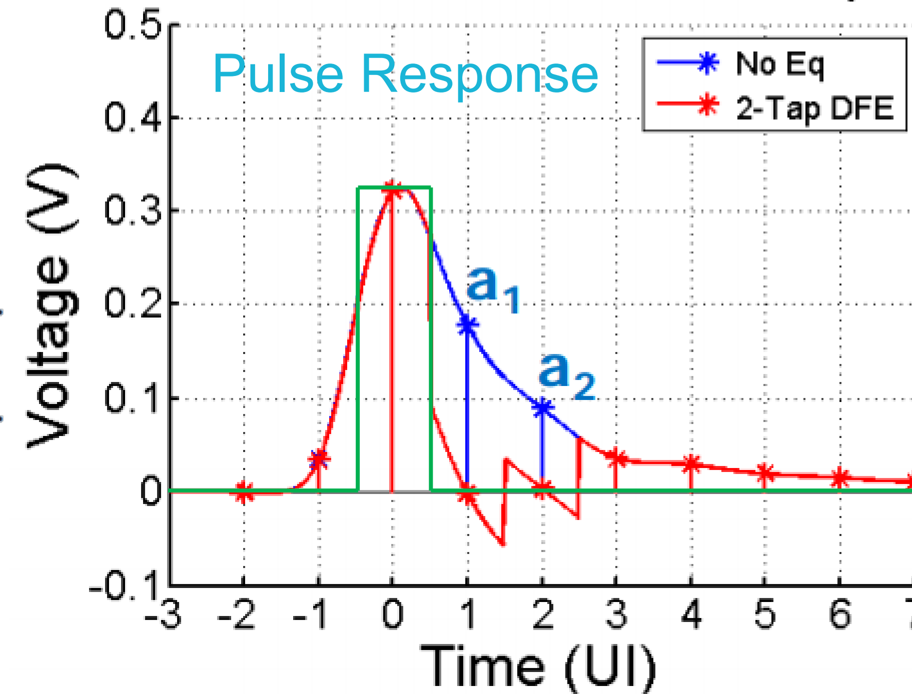
What Is Decision Feedback Equalization (DFE)?

PATTERN-RELATED EFFECTS CAN BE REDUCED BY SUBTRACTING-OUT KNOWN VOLTAGE SHIFTS BASED ON N-BIT PATTERN HISTORY

- Very good at reducing jitter caused by ISI and reflections

DFE Architecture





Summing the input with variable voltages (a1, a2, etc) for bit-wide durations after the cursor lets you attempt to piecewise interpolate a better approximation of an ideal 01000 pulse (green) from the actual pulse response (red/blue).

- 4-Taps of DFE are supported in DDR5

DDR5 Testing with DFE

NOT ALL DDR5 TESTS ENABLE DFE OPERATION

- DDR5 testing philosophy is to separate-out clock, data and pattern related issues
- Most tests are run with 111000111000 bit pattern to remove errors from ISI
  - DDR5 Uses a “by-four” interleave to achieve high-speeds
  - The “by-four” interleave means that a 3-1’s/3-0’s data pattern will give varied data to each interleave
  - During these tests, DFE is disabled
  - These tests include clock and data amplitude sensitivity and clock jitter sensitivity
- Only stressed-eye testing uses DFE
  - Stressed-eye testing operates the full digital receiver and measures BER in resulting decisions

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How to Know What Bit Decision a Receiver Makes?

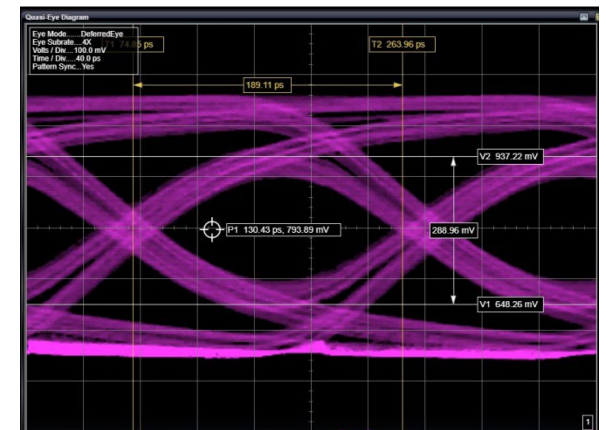
A LOOPBACK PATH IS IMPLEMENTED IN DDR5

- Loopback allows a receiver to send real-time decision results to a test system
- Loopback is a single, shared wire that can be selectively driven by any receiver
- Because it is so widely shared, it has very poor signal integrity
  - Quarter- or Half- rate speeds give more time for clean loopback operation
- Loopback features are not technically required in Memory Controller applications
  - But memory controllers who do not implement loopback features have Rx test challenges

Measurements We Can Make Using Loopback

THERE IS A LOT YOU CAN DO IF YOU HAVE QUARTER- OR HALF-RATE LOOPBACK OF REALTIME BIT DECISIONS

- Bit Error Rate
  - Fixed pattern and PRBS patterns that are looped-back can be synchronized to using BERTs
  - BERTs can measure bit error rate
- By skewing the timing of DQ versus DQS (or REFCLK versus CA lane) we can scan the horizontal opening margin
  - BER Bathtub Curve
- By skewing the horizontal timing <u>and</u> sweeping vertical DQ voltage offset, we can map-out an Eye Diagram
  - “Deferred Eye™” -- view at the actual bit decision point deep inside an IC
  - Best way to determine eye opening
  - Visual way to determine frequency response of on-die processing

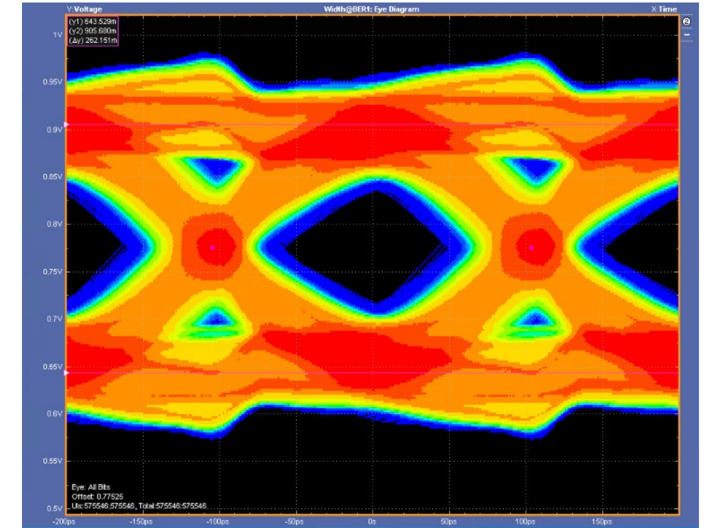


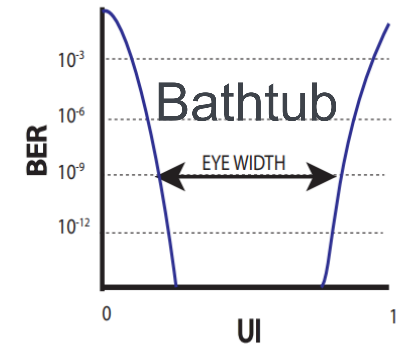
Bit Error Rate Bathtub Curve

WHAT IS IT?

- Y-axis is the measured Bit Error Rate level versus …
- X-axis is the DQ to DQS timing delay offset
- Practical BER measurements are limited by the amount of time it takes to observe enough bit decisions
- BER Bathtub curves typically measure down to a prescribed level and then extrapolate down to a deeper level.
- DDR5 BER performance is evaluated at $1x10^{-16}$ level
- The Bathtub plot shows the width of the eye opening down to different BER levels

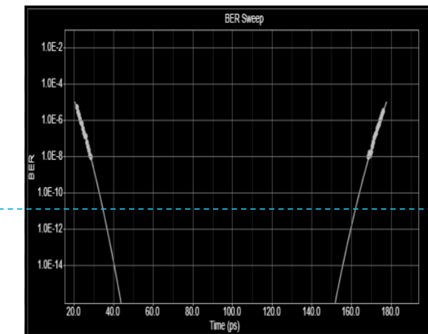
“Bathtub” Analysis show BER Margin





Measure

Extrapolate



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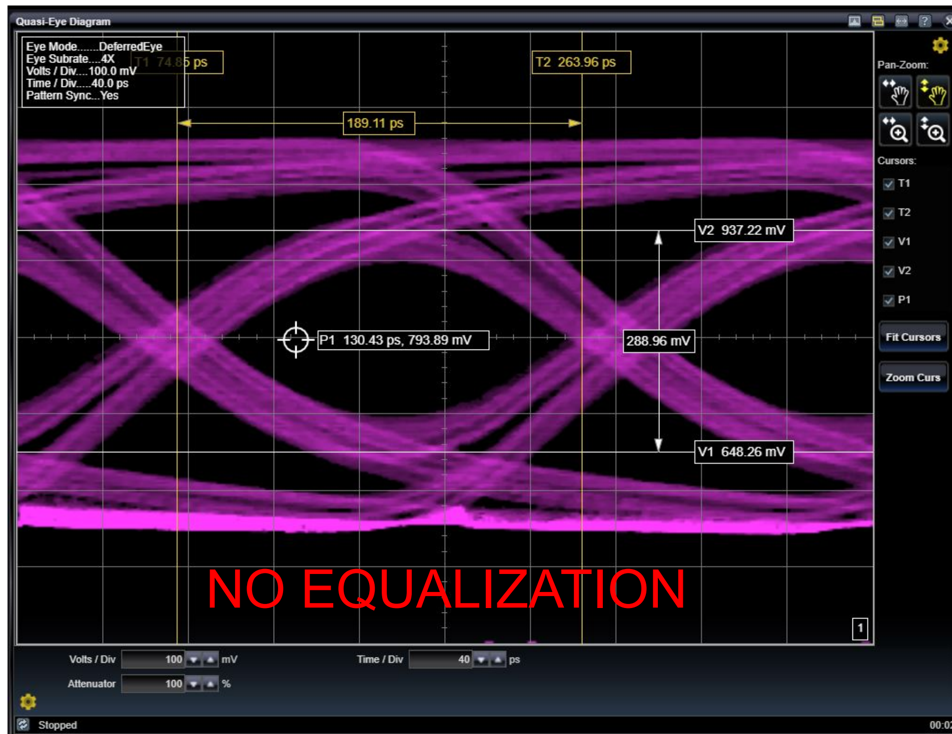
Deferred Eye™ Diagram at Slicer Input

IT'S POSSIBLE TO SEE WHAT THE EYE LOOKS LIKE RIGHT AT THE SLICER (WITHOUT SIMULATION)

- With support from Pattern Generator, deferred analysis can forward slicer decisions out the LOOPBACK signal to measure the Deferred Eye™ diagram from inside the Rx chip



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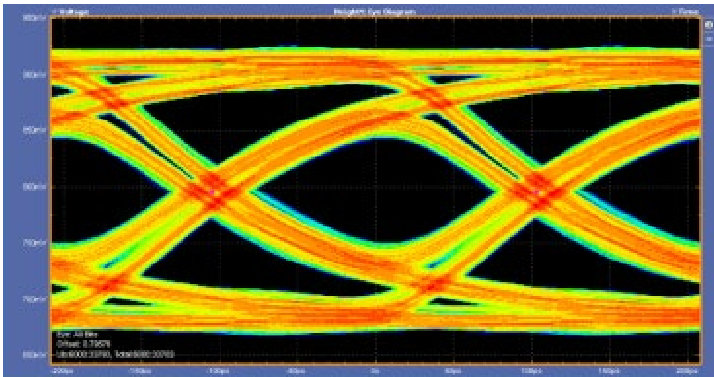
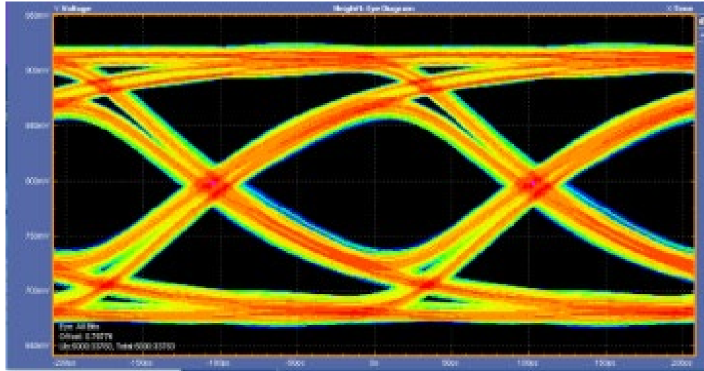
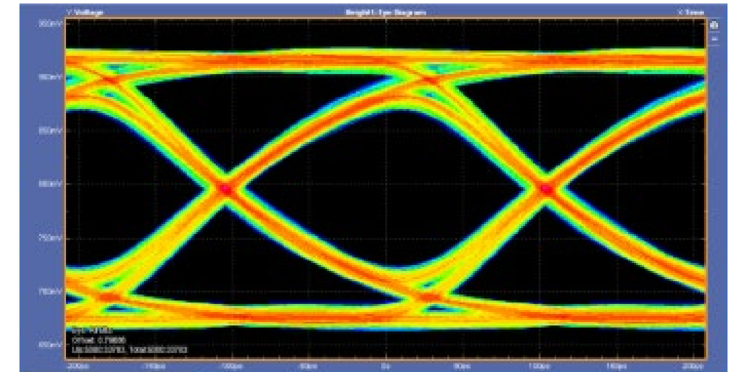
Correlating Deferred Eye™ Measurement with Scope

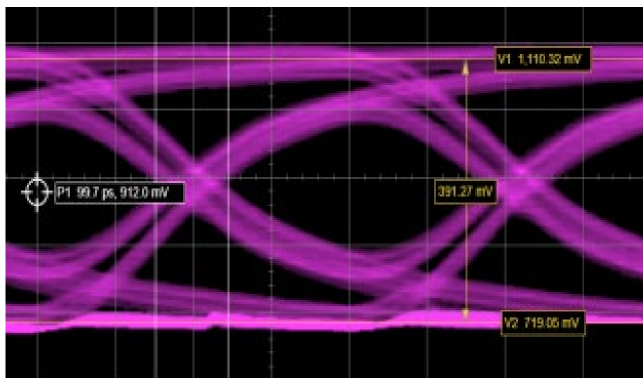
SCOPE EMBED/DE-EMBED MODELING CAN BE CHECKED AGAINST RX SLICER EYES

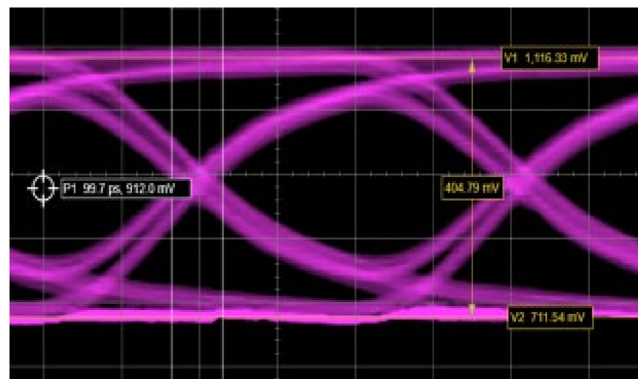
- 3 Test cases with various amounts of ISI for Oscilloscope/Deferred Eye™ correlation
  - Used to understand/validate package models

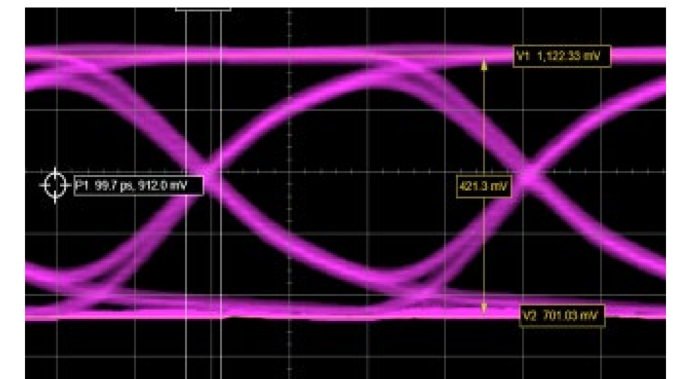












Testing Depends on a Flexible Pattern Generator

PATTERN GENERATORS CREATE TEST PATTERNS WITH KNOWN IMPAIRMENTS

- Programmable Pattern Generators support
  - Variable data rates
  - Variable signal amplitudes and offsets
  - Variable jitter (sinusoidal, random, DCD)
  - Variable vertical stress (sinusoidal interference)
  - Multiple channels (for DQ, DQS and Refclk)
  - I2C interface to registers inside DUT
- Even with calibrated Pattern Generators, new in-system re-calibrations must be done
  - Accounts for cabling and test boards
  - For example:
    - Sine interference at the front of the Pattern Generator is not the same as the sine interference at the input of the DDR5 Receiver because of losses in the cabling and test boards.

Testing Also Depends on a Deep Memory Scope

MUST USE DSP TO IMPLEMENT DDR5 REFERENCE RECEIVER FOR TEST PLATFORM CALIBRATIONS

- Deep memory scopes are needed for the calibration phase
- Bandwidths of 13 GHz are used
- Scopes use embed/de-embed filters based on S-parameters to move reference plane of measurement
  - Reference plane is the input to the bit-decision flip flop inside the IC for Stressed-Eye tests
  - Reference plane is the ball of ICs for all other tests
- Embed/De-embed adds/removes wanted/unwanted portions of a measurement

Two Measurement Reference Planes Are Used

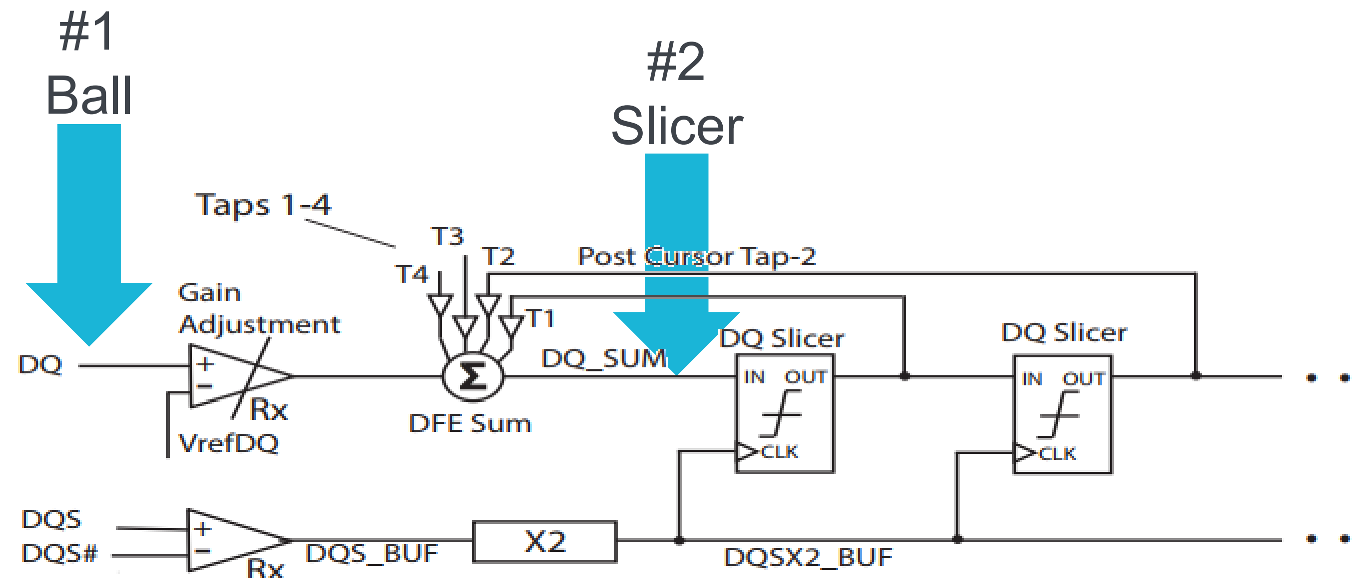
REMOVES DEPENDENCY ON EQUIPMENT, CABLES AND TEST BOARDS

Used for all other stress calibrations

Used for Receiver Stressed-Eye opening calibration

#1 Ball

#2 Slicer



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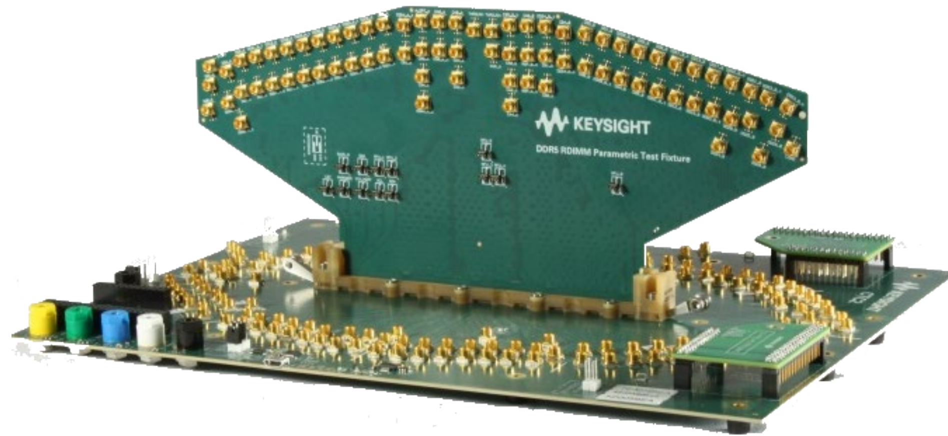
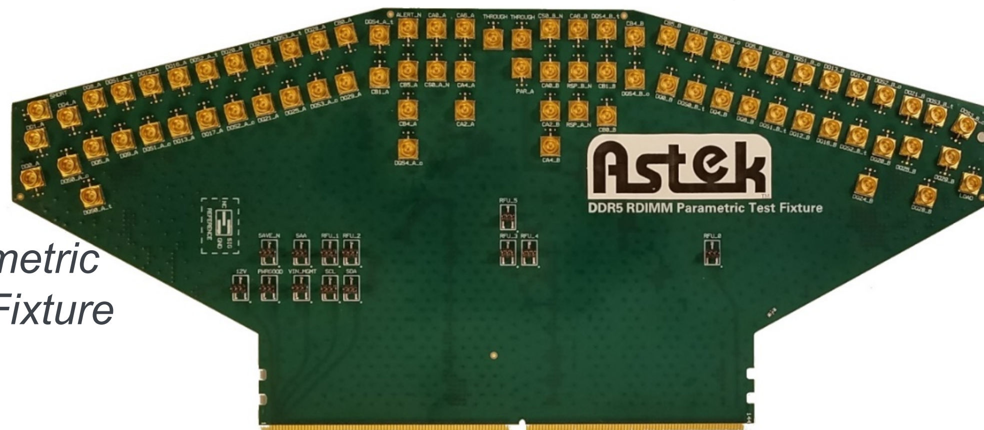
Test Platform for RDIMM, LRDIMM Modules

REGISTER CLOCKING DEVICES (RCD) ARE PRESENT ON THESE MODULES

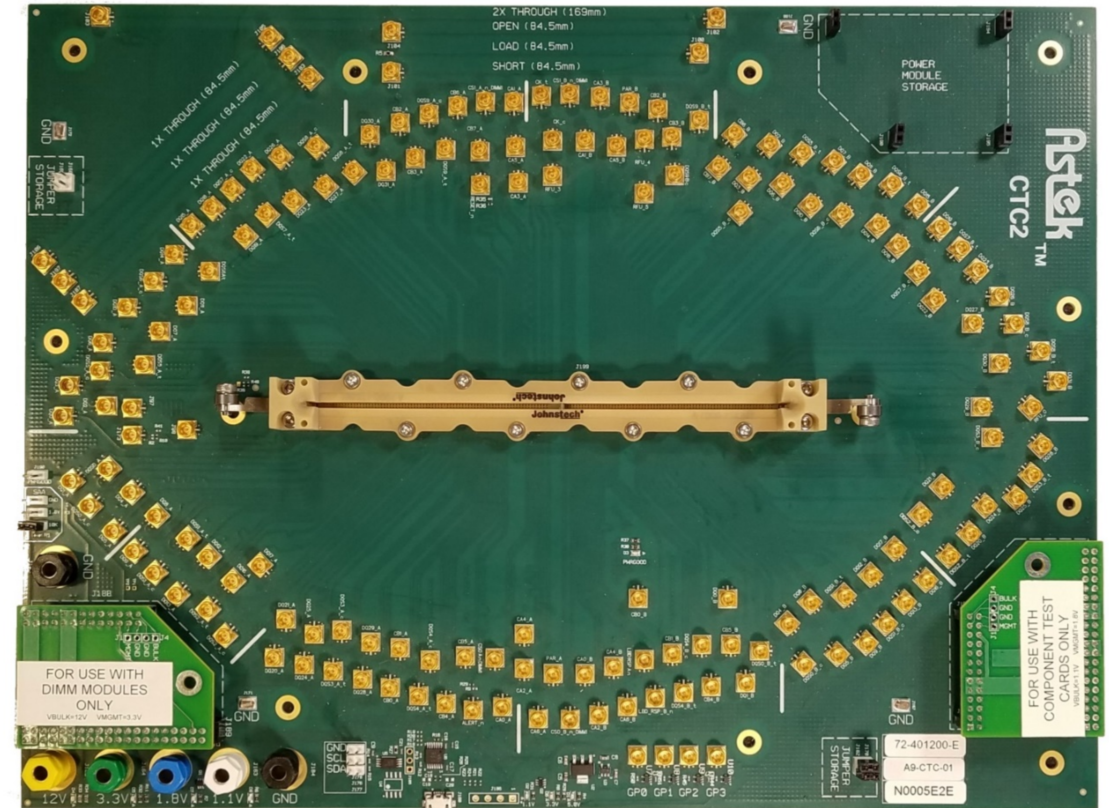
JEDEC-Designed test boards available from Astek





Parametric Test Fixture (PTF)

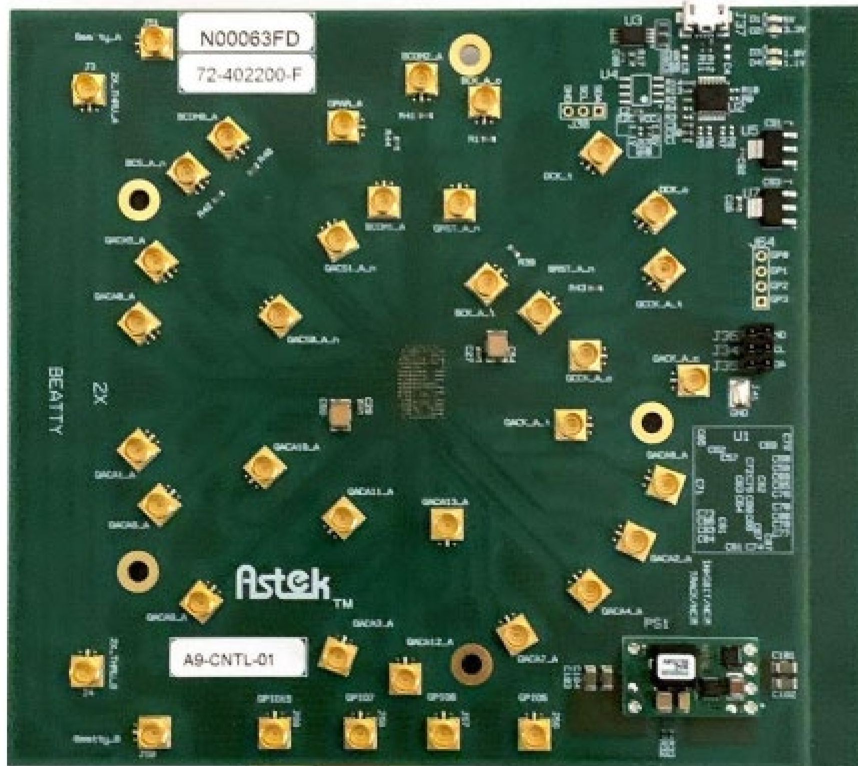
CTC2 Test Fixture



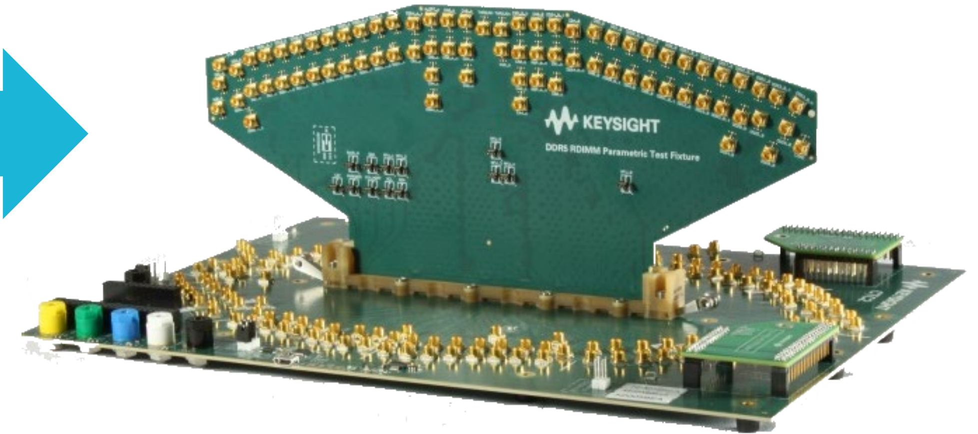
ALSO USED FOR COMPONENT-LEVEL TESTING

Test Platform for Other Modules

WHEN AN RCD IS NOT PRESENT, AN EXTERNAL RCD-DEVICE CAN BE USED

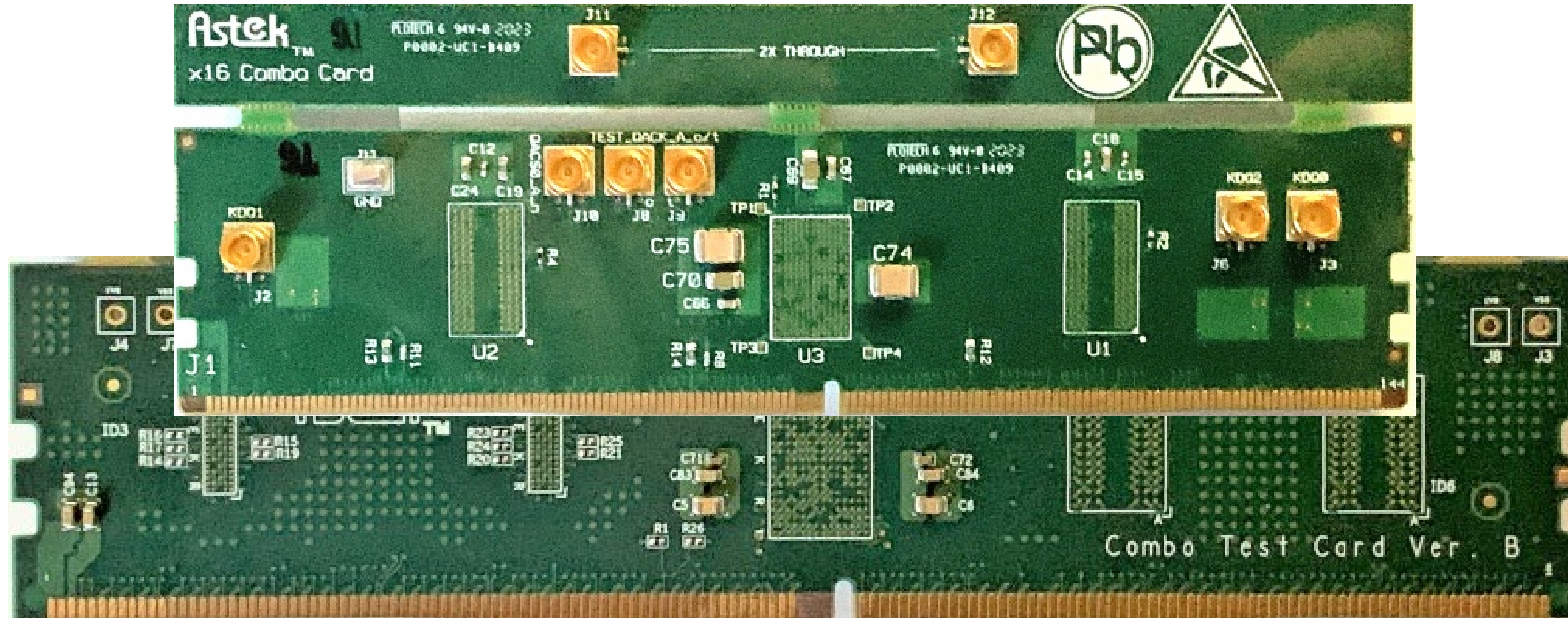


18 SMA Cables provide CA lanes from test RCD to the CTC2 board to communicate directly to DRAM ICs.



Device Test Support

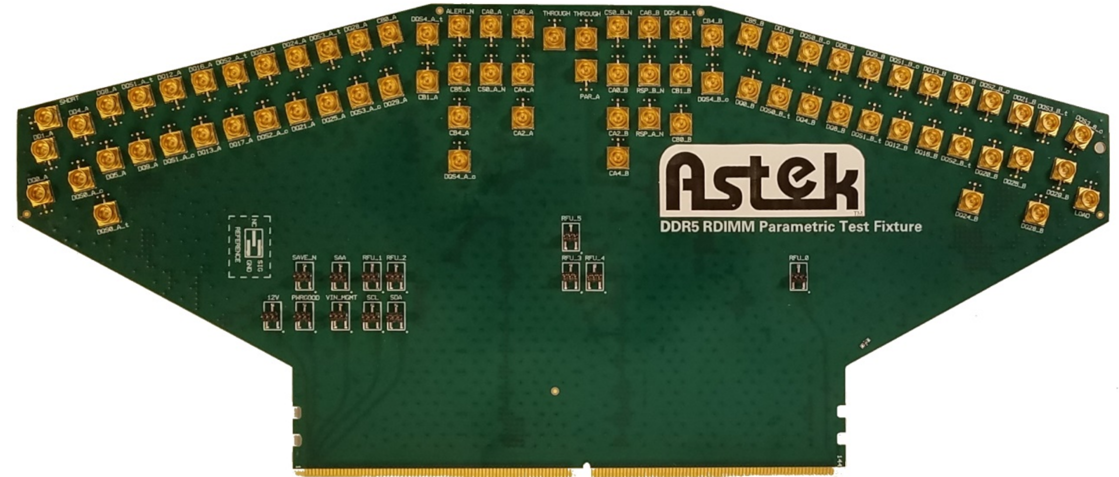
ASTEK ALSO SUPPLIES COMBO TEST CARDS FOR USE IN CTC2



Test Platform for Memory Controllers

MEMORY CONTROLLER TEST CONFIGURATIONS WILL DEPEND ON THE APPLICATION

- Parametric Test Fixture provides SMP connectors for all I/O
- Stimulate Controller receivers by driving DQ lanes from Pattern Generator in response to DQS or REFClk
- Add stressors to DQ



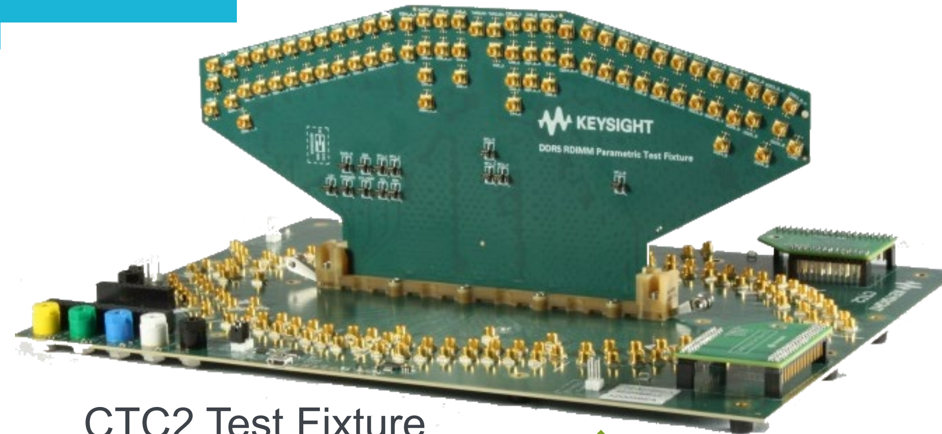
DDR5 Module Test System

PUTTING IT ALL TOGETHER

Deep Memory
Oscilloscope

DQS+
DQS-
DQ

Parametric Test Fixture



CTC2 Test Fixture

LBD

Pattern Generator
With Loopback
Error Detector

DQS+
DQS-
DQ
RefCLK+
RefCLK-
I2C BUS

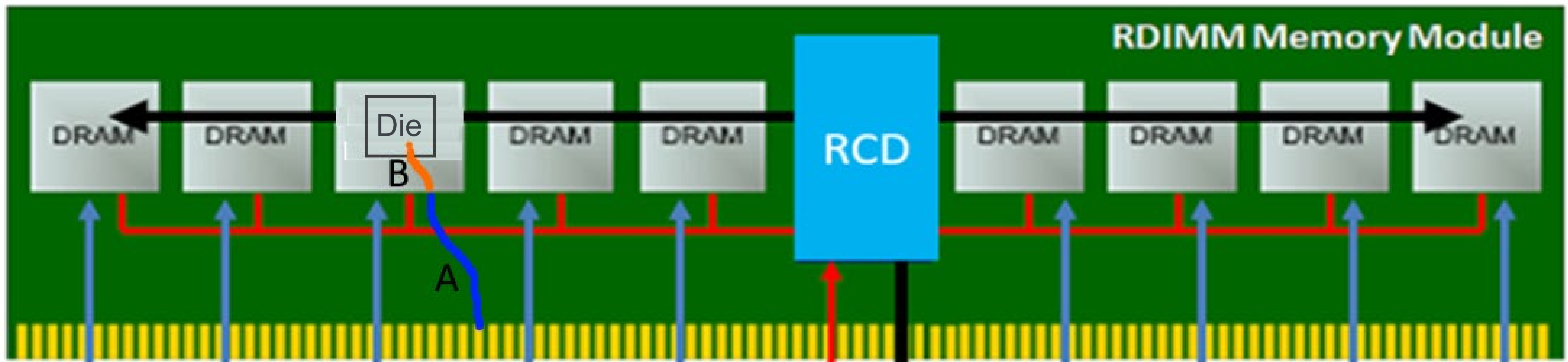
Also needed
For TX Testing

- Scope needed for TX Test and during RX system calibration
- New System Calibrations when?
    - Change in data rate
    - Change in data lane
    - Change in cabling
- Databased calibrations makes this easy

Embed and De-Embed Is Necessary for DDR5 Test

MEASUREMENT POINTS DON'T ALIGN WITH PROBING POINTS

- Some loss as been added into the measurement and should be removed (De-embed)
  - Scope cables, SMP connectors, extra PCB trace length
- Other loss has not been added into the measurement and should be added (Embed)
  - Correct PCB traces, Package and circuits up to the slicer point



- Must add (embed) A and A+B for the two reference planes…

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Measuring Losses in the Test System

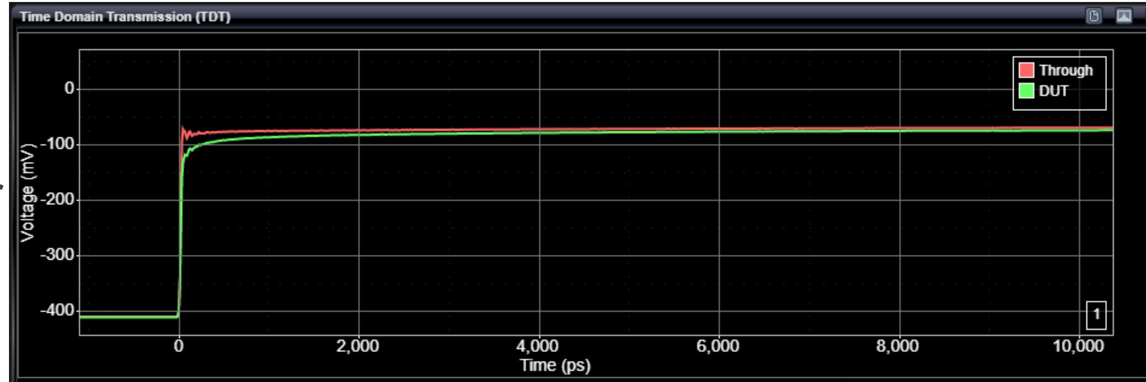
FREQUENCY DOMAIN AND TIME DOMAIN APPROACHES

- Insertion Loss (S21) and Return Loss (S11) are needed for DSP to correct for fixtures
- Using a Vector Network Analyzers (VNA) or Time Domain Analyzer (TDR/TDT)
  - VNAs send many sinewaves thru a DUT and measures amplitude & phase of response
  - TDT send a single fast-edged square wave thru a DUT and studies how it has changed
  - VNAs have high sensitivity but come with a high price
  - TDR/TDT works well in lower-loss measurements and are more affordable
- For DDR5, both single-ended and differential measurements are needed
  - Measurement bandwidth needs to be > 13 Ghz
- Both devices output Touchstone files used by oscilloscopes

Time Domain Transmission for S-Parameters

COMPARING A FAST EDGE BEFORE AND AFTER TEST DUT…

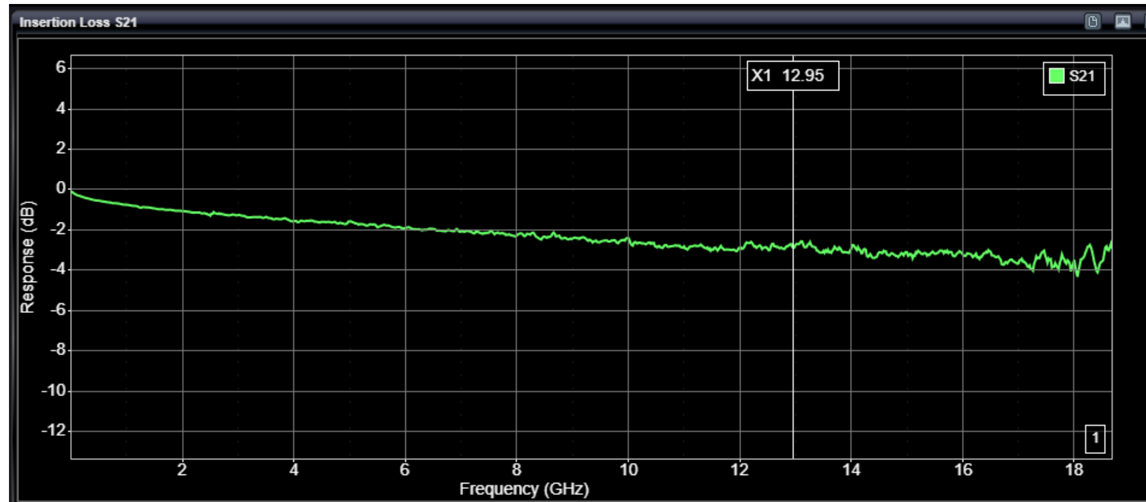
TDT
Before/After



Time →

Ratios of Spectrums gives frequency dependent loss

Insertion
Loss (S21)



Frequency →

Touchstone .S1P file

```
! STEPSCOPE S21 S1P FILE
!
! Version,1
! DateTime,Sat Jan 18 14:18:54 2020
!
! OFFSET,0.000000,GHz
! SPAN,20.020000,GHz
! COUNT,1001
! PERSISTENCE,1
! AVERAGES,1
!
! Option line
# GHz S DB R 50

! FreqGHZ   S21_dB    S21_Angle

0.000000 -0.107478   0.000000
0.020000 -0.126463   -0.698566
0.040000 -0.171307   -0.873690
0.060000 -0.210967   -1.038736
0.080000 -0.234628   -1.219661
0.100000 -0.265780   -1.317766
0.120000 -0.283124   -1.434097
0.140000 -0.305072   -1.519987
0.160000 -0.317864   -1.636151
0.180000 -0.338647   -1.710833
0.200000 -0.352346   -1.772180
```

How Important Is It to Have S-Parameters?

EXAMPLE OF EYE HEIGHT MEASUREMENT WITH 1DB ERROR AT THE BIT RATE FOR STRESSED-EYE CALIBRATION

- A High Frequency 1010 pattern suffers more loss than a slow 11111110000000 pattern
  - 1010 frequency is DATARATE/2 (e.g. 2.4GHz for a 4.8Gbps speed)
  - A typical system loss at 2.4GHz is -2 dB (20% loss)
- Compare eye height with -2dB loss to one using a -3dB loss (30% loss)

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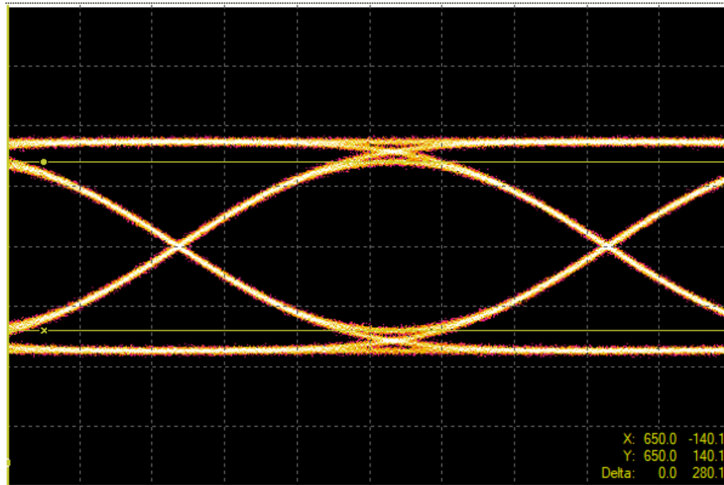
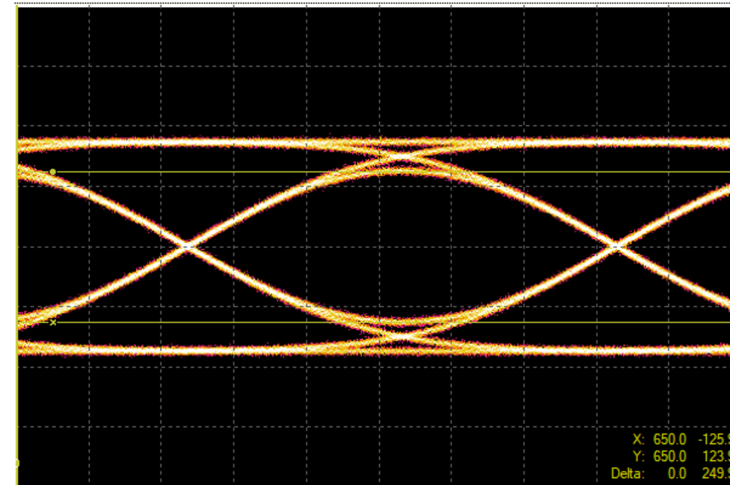
What's 1dB?

10% DIFFERENCE IN S21 TRANSLATES TO A 30% DIFFERENCE IN EYE HEIGHT

-2dB @ 2.4GHz

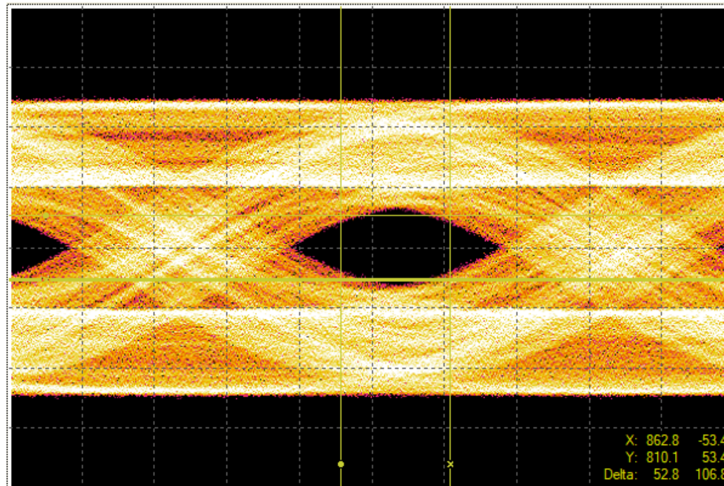


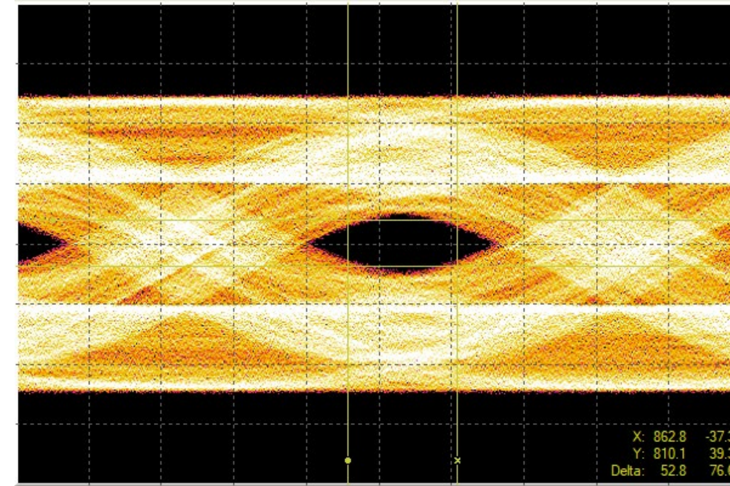


-3dB @ 2.4GHz

Stressed-Eye
106 mV EH

Includes SI, SJ, RJ





Stressed-Eye
76 mV EH

Calibrated Stressed Eyes would wrongly inject more stress to achieve target eye height

More parts would fail!

Estimating S-Parameter Models

WHEN S-PARAMETERS ARE NOT SUPPLIED BY THE VENDOR, GOOD ESTIMATES CAN BE MADE

- S-parameters for the on-die signal processing between the ball of a chip and the input to the D-flip flop cannot be measured directly
  - Vendors could supply simulation results; however, this may be difficult to get
- Deferred Eye Diagrams uses the DDR5 sampling flip-flop to give a view at the Eye Diagram it sees
  - It is easy to see the response at DATARATE/2 and at low frequencies
  - These must be compared to embed/de-embed measurements at plane #1
- With this single data point, a simple low-pass filter model can be created
- By changing to different speeds more model points can be measured
    - 3.2, 4.8, 5.4, 6.4 Gbps yields S21 data points for 1.6, 2.4, 2.7, 3.2 GHz

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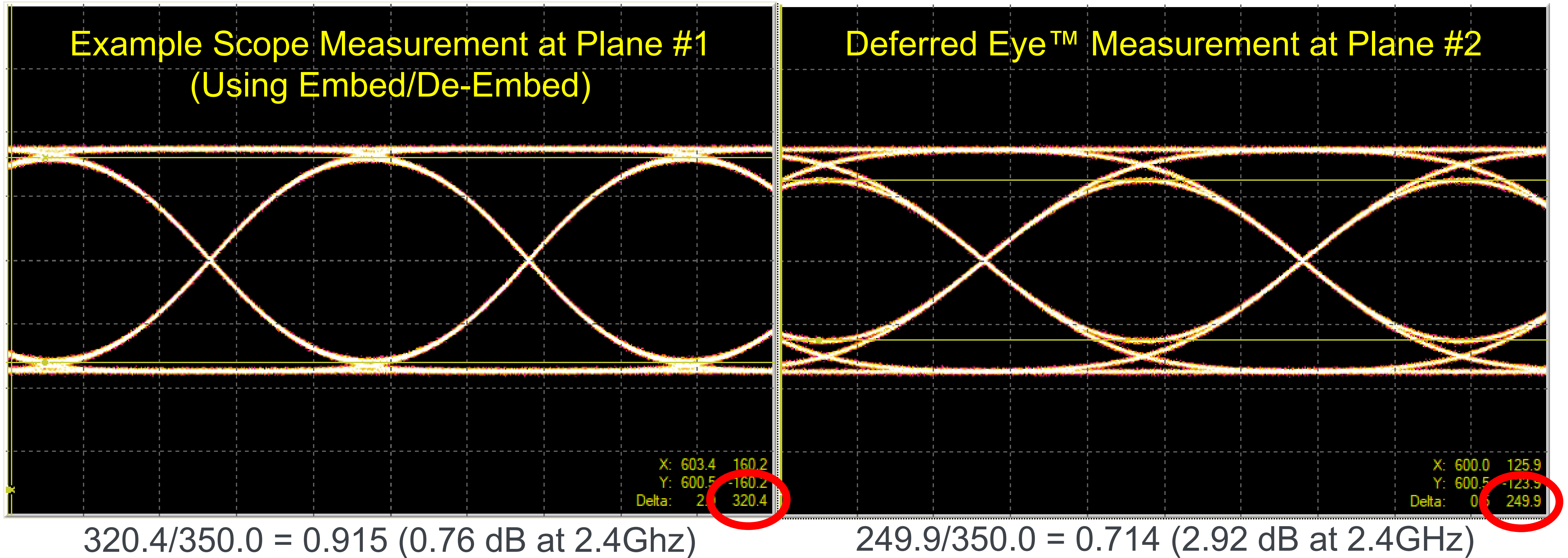
Estimating S21 Inside IC

ESTIMATE OF LOSS AT DATARATE/2 IS MADE BASED ON ADDITIONAL LOSS BETWEEN PLANE #1 AND PLANE #2 USING 350MV SIGNAL



320.4/350.0 = 0.915 (0.76 dB at 2.4Ghz)

249.9/350.0 = 0.714 (2.92 dB at 2.4GHz)

"Additional" Loss is 2.92 – 0.76 = 2.16dB @ 2.4GHz from "Inside IC" path

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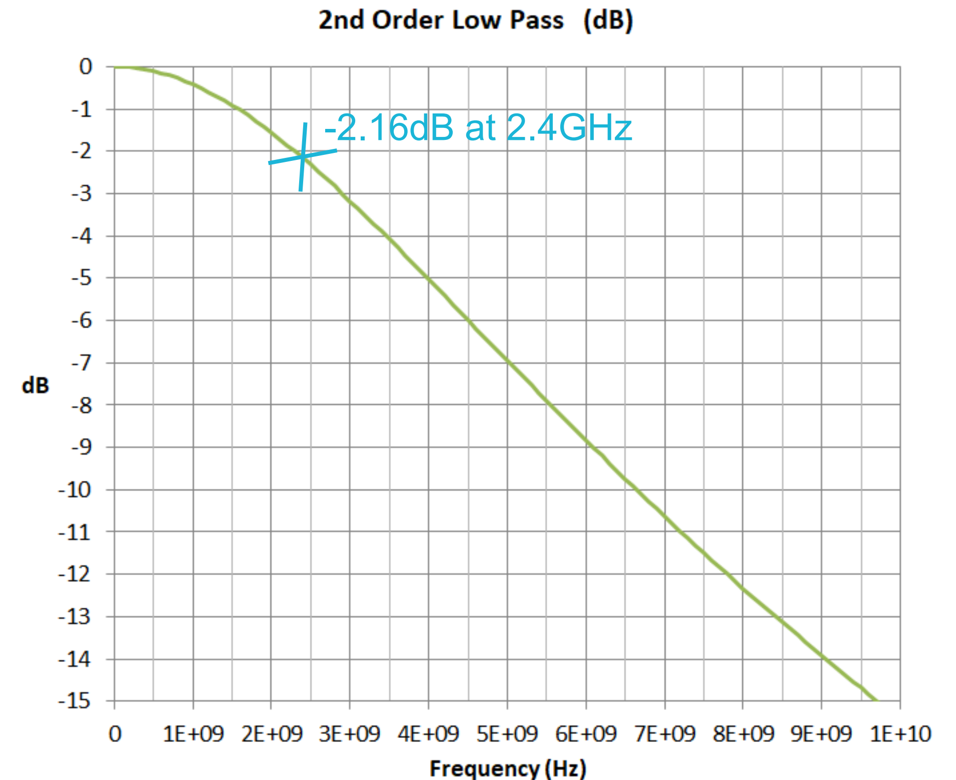
Using a 2nd-Order Low Pass Filter We Compute S21

DRAW A 2ND-ORDER LOW PASS FILTER THROUGH THE MEASURED POINT(S)

```
! S21 S1P FILE (Excel Generated)
! 2 Order RC Filter Response
! -1.04dB loss at 1.6 GHz
! -2.18dB loss at 2.4 GHz
! -3.2dB loss at 3 GHz
!
! Version,1
# GHz S DB R 50
! FreqGHZ S21_dB S21_Angle
0 0 0
0.1 -0.0043 -2.55
0.2 -0.0172 -5.1
0.3 -0.0386 -7.64
0.4 -0.0686 -10.17
. . .
2.2 -1.8666 -52.18
2.3 -2.0214 -54.21
2.4 -2.1801 -56.22
2.5 -2.3426 -58.18
2.6 -2.5086 -60.11
. . .
12.8 -19.1955 -141.31
12.9 -19.3159 -141.59
13 -19.4357 -141.87
```

-2.16dB at 2.4GHz →



Test System Calibrations

CREATING ACCURATE TEST SIGNALS AT REFERENCE PLANES USING TEST FIXTURES AND CABLES

- DQ, DQS+/DQS-, CA and RefCLK+/RefCLK- stimulus needs to be calibrated
- Scope and PTF is used with Embed/De-Embed and reference channel
- Calibrations at reference plane needed for:
  - Amplitude,
  - Jitter (Random, Sinusoidal, Duty-Cycle Distortion)
  - Sinusoidal Interference
  - Stressed-Eye Settings (must use DFE)
- Calibrations can be different for different lanes and speeds
- Automation can make this a one-button push

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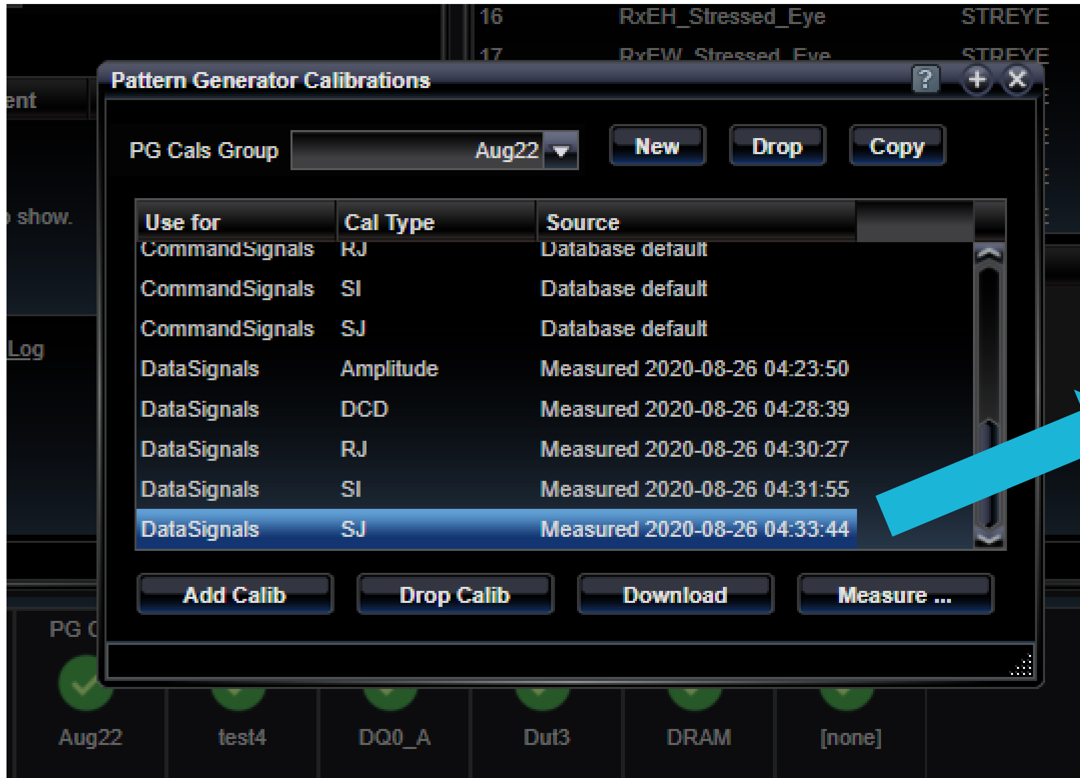
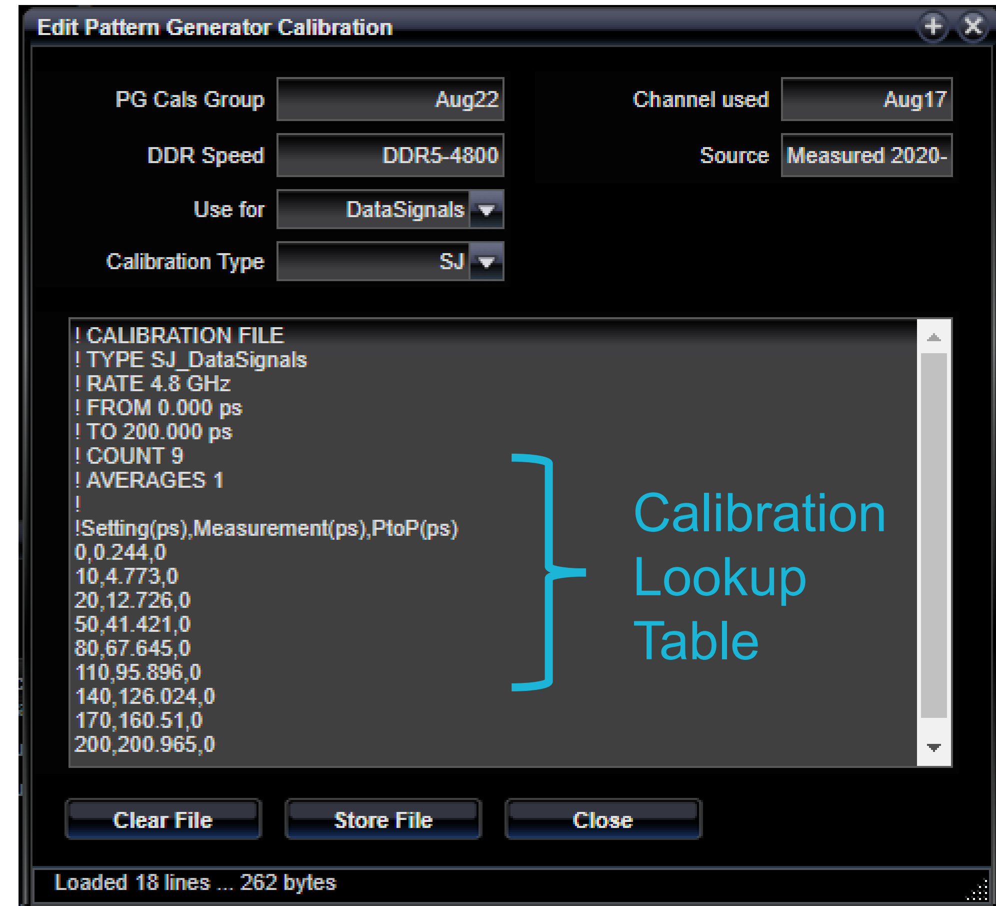
Example Pattern Generator Calibration

RANDOM JITTER

All the various different Pattern Generator Calibrations
For different signal types





Example Stressed-Eye Calibration

COCKTAIL OF STRESSORS THAT CAUSE DESIRED EYE OPENING

Both DQ Data Lanes and Command Lanes can have Stressed-Eye calibrations

Stressed Eye Calibrations

Stress Cals Group: test4 | New | Drop | Copy

Use for	Calib	S Parameters	Source
CommandLanes	Default	Default	(use Measure button)
DataLanes	Aug22	Aug17	Measured 2020-08-26 04:52:52

Add Eye Cal | Remove | Algorithm | Measure ...

Stress: test4 | DQ0_A | Dut3 | DRAM | [none]

Algorithm for how to add stressors can be configured

Edit Stressed Eye Calibration

Stress Cals Group	test4
DDR Speed	DDR5-4800
Use for	DataLanes
Channel used	Aug17
PG Cals used	Aug22
DFE Taps used	-20, -5, -5, -5
DFE Gain used	0dB

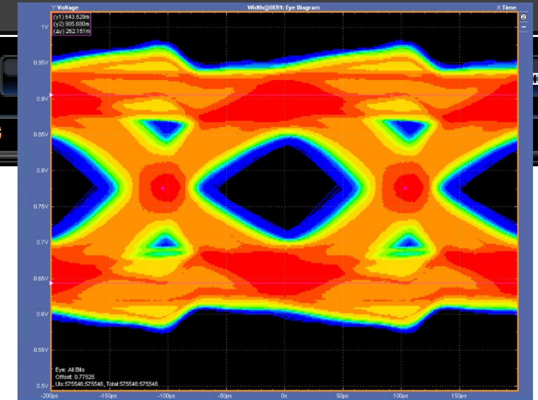
RJ	0.006	UI rms
SJ	0.001	UI
SI	125	mV
Amplitude	271	mV
Result EW	0.25	UI
Result EH	70.526	mV

Source: Measured 2020-08-26 04:52:52

Log:
Final EW Measurement: EW=0.252 UI, Target was 0.250 UI, Error is 0.8%
Final EH Measurement: EH=70.5 mV, Target was 70.0 mV, Error is 0.8%
Measured 2020-08-26 04:52:52
Stressed eye calibration successful
7.5 minutes

Clear | ...ose

95 lines ... 4,079 bytes

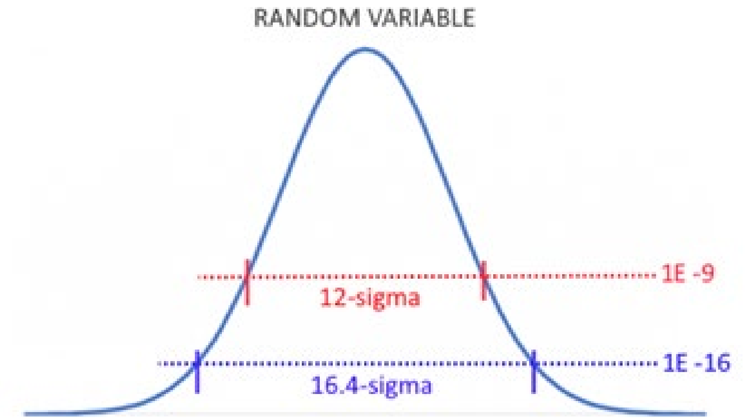


Resulting Scope Eye

One Detail for Stressed-Eye Calibrations

DESIRED EYE HEIGHT AND EYE WIDTH ARE SPECIFIED AT BER OF $1X10^{-16}$

- However, reasonable scope measurements used during calibration can get to a BER of $1x10^{-9}$
- Random effects will increase going from $1x10^{-9}$ to $1x10^{-16}$ by 4.4σ
- Because the test signals come from a pattern generator, we know what RJ was injected so we can adjust our Eye Width measurement
- Eye Height measurements are much less impacted going from $1x10^{-9}$ to $1x10^{-16}$ as vertical stress is much less random



After All Calibrations Are Complete…

ITS TIME TO START ACTUAL DDR5 CONFORMANCE ANALYSIS

- There are 4 DDR5 conformance analysis
  - Data Voltage Sensitivity
  - Clock Voltage Sensitivity
  - Clock Jitter Sensitivity
  - Stressed-Eye Performance
- All analysis are based on the fundamental “BER Bathtub” measurement on the loopback signal
  - Display measured BER versus delay offset between DQ/DQS or CA/RefCLK

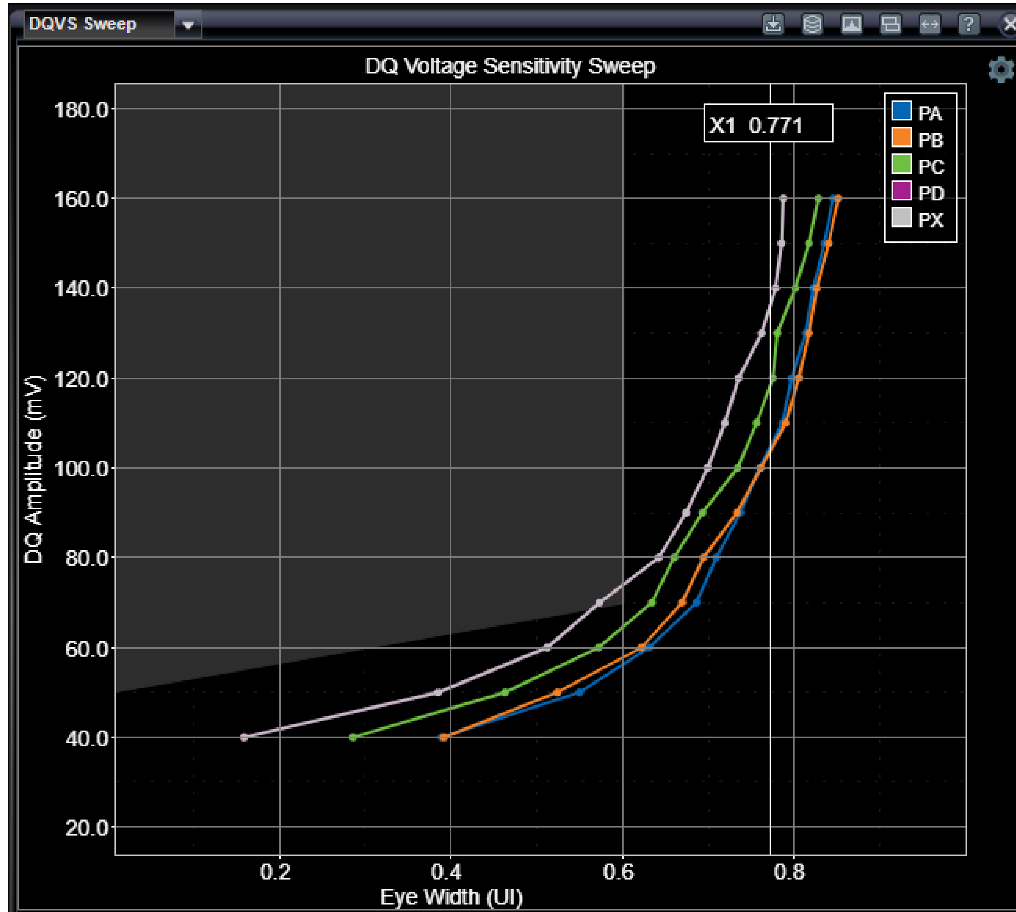
DDR5 Rx DQ Voltage Sensitivity

CHECK THAT BITS ARE RELIABLY DETECTED WHEN DQ AMPLITUDE IS SMALL

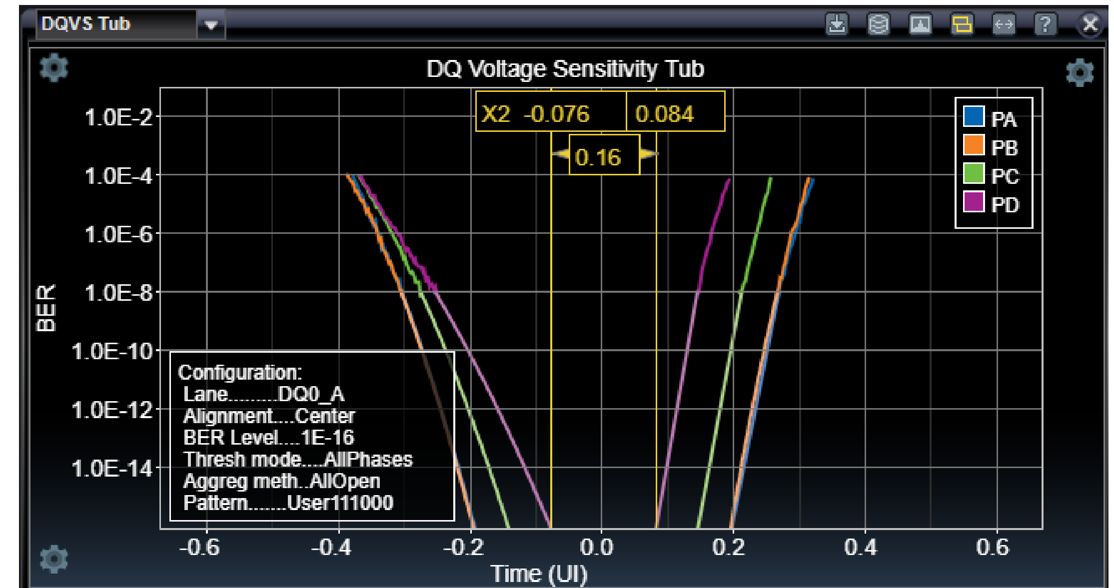
- Non ISI-pattern (111000) is used when testing Voltage Sensitivity Compliance
  - Testing with PRBS patterns is useful for characterization
- Individual interleaves phases can be tested separately and/or aggregated
- No Rx Gain or DFE used
- Measure BER Bathtub curves for each phase at each DQ amplitude setting
- Decrease DQ amplitude eye width margin goes to zero

DQVS “Deep Dive” Example

DQVS PLOTS SHOW VOLTAGE SENSITIVITY FOR EACH OF 4 PHASES



Points for each amplitude is the result of a BER Bathtub analysis on all 4 phases



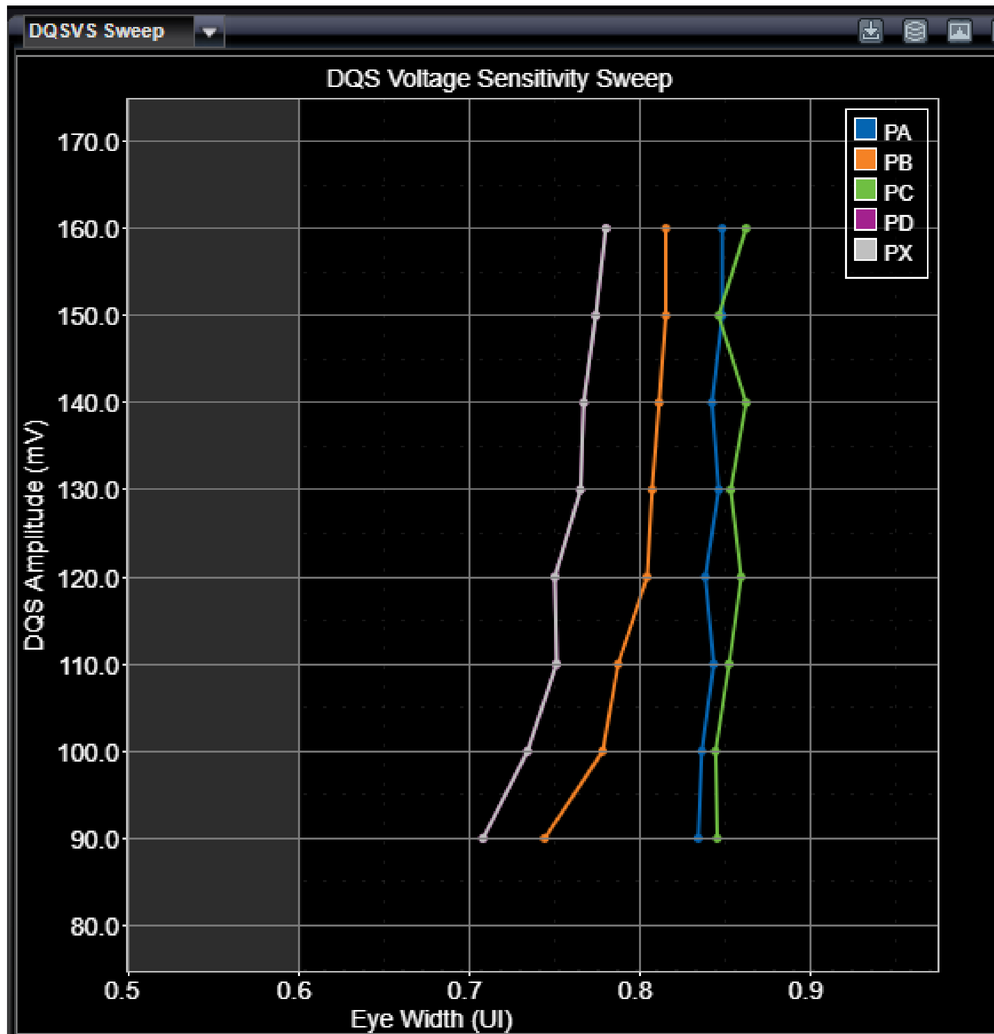
DDR5 Rx DQS Voltage Sensitivity

SIMILARLY, CHECK THAT BITS CAN BE DETECTED WHEN DQS CLOCKING IS SMALL

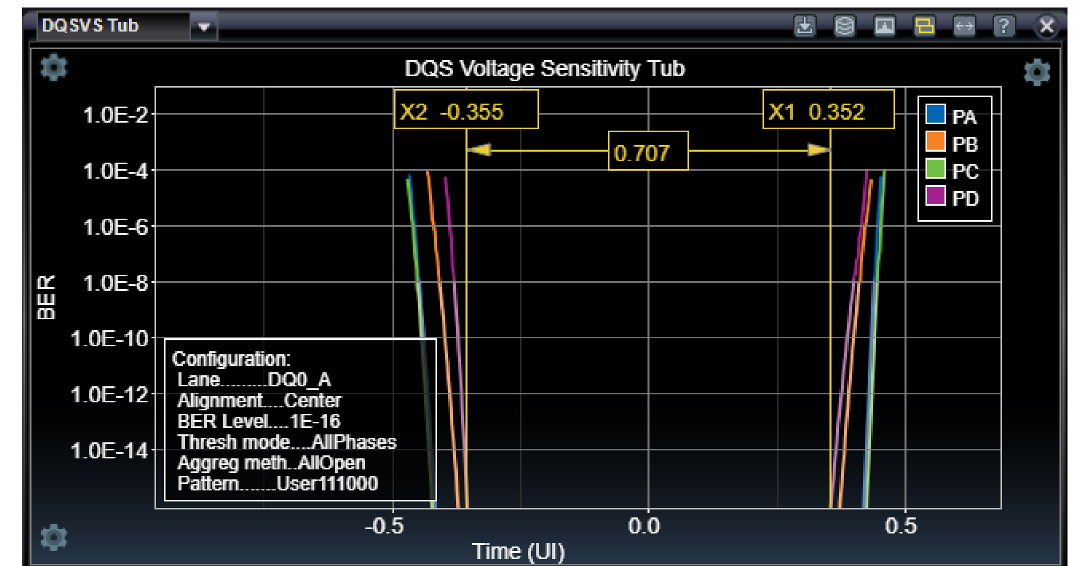
- Clock patterns are always 1010 to make a double data rate clock
  - PRBS test patterns can also be helpful
- As clock amplitudes drop, data lanes will no longer be able to accurately sample bits
  - This is measured with a BER Bathtub analysis
- This test lowers the DQS amplitude until no extrapolated eye margin is present
- Each phase may have different DQS sensitivity, so it is best to check all 4 phases

DQSVS "Deep Dive" Example

DQSVS SHOWS VOLTAGE SENSITIVITY TO DECREASING DQS AMPLITUDE



Again, Points for each amplitude is the result of a BER Bathtub analysis on all 4 phases



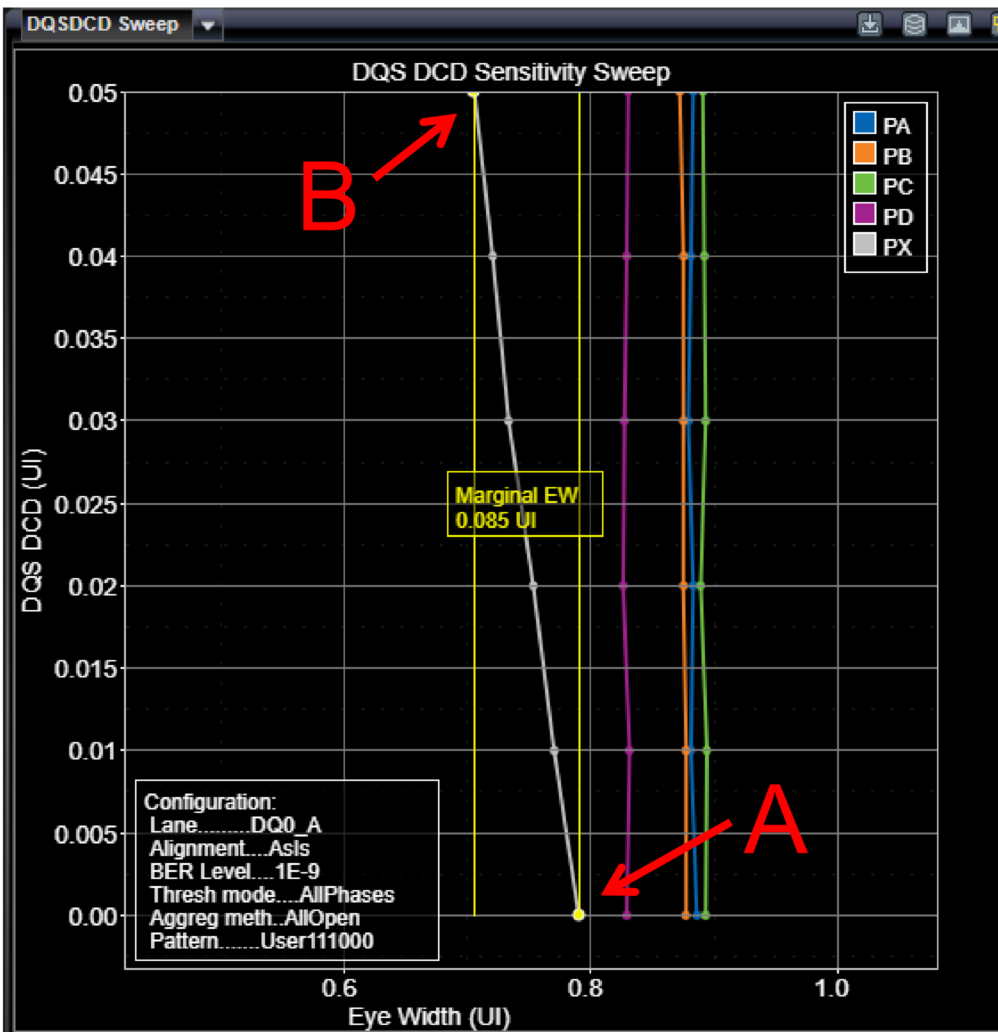
DDR5 Rx DQS Jitter Sensitivity

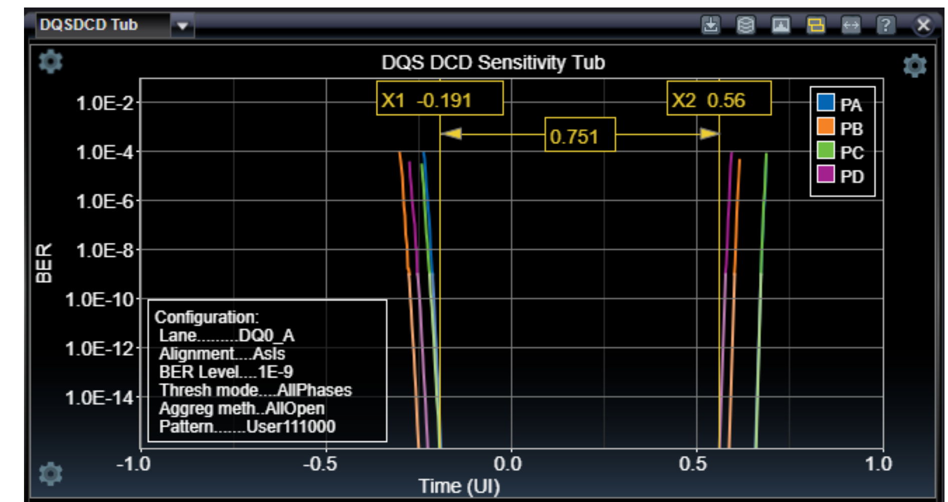
TEST THAT BITS CAN BE DETECTED WHEN JITTER IS PRESENT ON DQS CLOCK

- Clocking sensitivity compliance tests are done without ISI (111000 pattern)
- Three types of jitter profiles are inserted onto the DQS during this test
  - Duty Cycle Distortion (DCD)
  - Random Jitter (RJ)
  - DCD + RJ
- Jitter Sensitivity tests measures the decrease in eye width margin caused by jitter
  - Meant to test for abnormal clock jitter multiplication
- Measurements with no jitter is first used to establish the baseline eye width margin
- All measurements made down to a BER of 1E-9 (quick measurements)

DQSJS “Deep Dive” Example

DQSJS SHOWS HOW ADDED CLOCK JITTER MAY GET MULTIPLIED IN A SYSTEM





Again, all measurements are based on using BER Bathtub analysis

A measures Eye opening with no injected jitter
B measures Eye opening with ALL injected jitter
B-A is the “decrease” in Eye opening from Jitter

Decrease should roughly match what jitter was injected—and not multiply it

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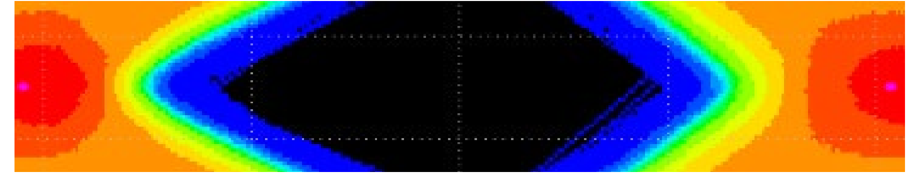
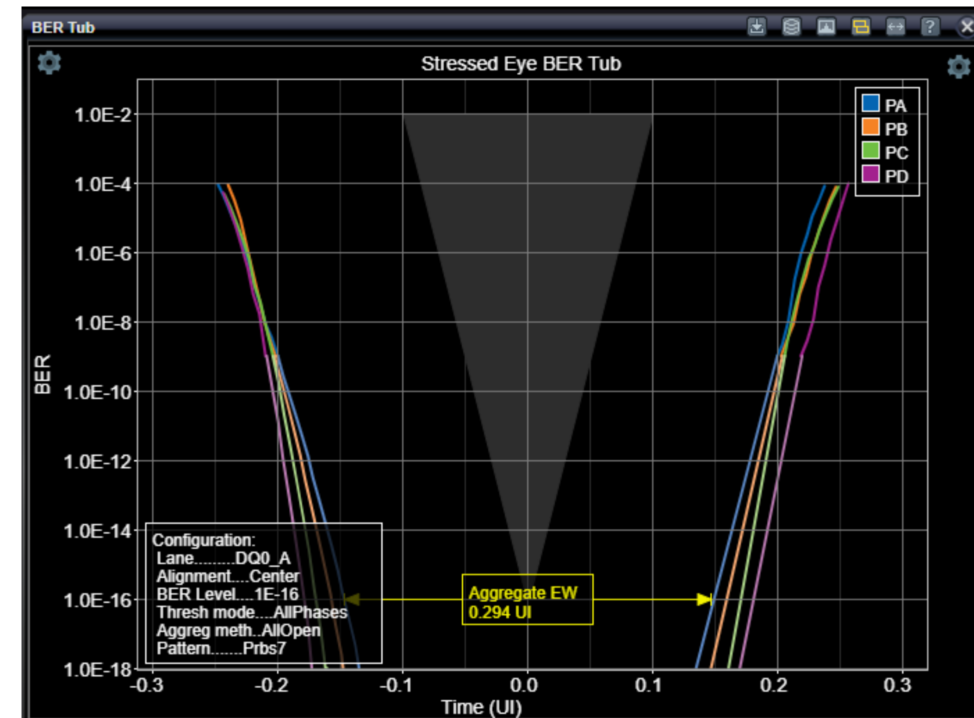
DDR5 Rx Stressed Eye Test

CHECK THAT BITS CAN BE DETECTED WITH COMPROMISED DATA

- Adjust Amplitude, RJ, SJ and SI for target eye opening
  - Rx DFE Equalization is set to match values determined by oscilloscope during calibration step
- BER Eye margin is measured using calibrated eye stimulus
- Calibration plane is at input to the slicer
  - On-Die S21 model is needed
- Result is a Bathtub curve showing available margin





"Deep Dive" Versus "Conformance" Testing

CONFORMANCE-ONLY TESTS ALLOW FOR QUICK LIMIT-ONLY TESTS

RX Test

Item	Symbol	Test	Criteria	Value	State	Audit
1	VRx_DQS	DQSVS	@ 100 mV	100 mV	Pass	BER=1E-16; Conf=99.00; Conf_BER=1E-8; Patt=User111000; VClk=400.0
2	VRx_DQS_EW_at_BER	DQSVS	> 0 UI	0.766 UI	Pass	EwA=0.85; EwB=0.81; EwC=0.86; EwD=0.77; ThrA=926.25; ThrB=926.25; Th
3	VRx_DQS_Best_BER	DQSVS	<=1E-16 BER	0 BER	Pass	A 0.0e+00; B 0.0e+00; C 0.0e+00; D 0.0e+00; Align=Center; Patt=User11100
4	VRx_DQ	DQVS	@ 65 mV	65 mV	Pass	BER=1E-16; Conf=99.00; Conf_BER=1E-8; Patt=User111000; VDat=400.0
5	VRx_DQ_EW_at_BER	DQVS	> 0 UI	0.467 UI	Pass	EwA=0.53; EwB=0.53; EwC=0.47; EwD=0.47; ThrA=909.75; ThrB=909.75; Th
6	VRx_DQ_Best_BER	DQVS	<=1E-16 BER	1.64e-57 BER	Pass	A 1.7e-77; B 1.5e-70; C 6.5e-57; D 2.7e-61; Align=Center; Patt=User111000
7	Rx_DQ_tMargin	DQSJS	>= 0.825 UI	0.837 UI	Pass	A 0.90; B 0.89; C 0.91; D 0.84; ThrA 925.00; ThrB 925.00; ThrC 925.00; ThrD
8	dtRx_DQ_tMargin_DQS_DCD	DQSJS	<= 0.06 UI	-0.00155 UI	Pass	A 0.07; B 0.04; C 0.08; D -0.00; ThrA 925.00; ThrB 925.00; ThrC 925.00; ThrD
9	dtRx_DQ_tMargin_DQS_Rj	DQSJS	<= 0.09 UI	-0.0791 UI	Pass	A -0.02; B -0.03; C -0.01; D -0.08; ThrA 925.00; ThrB 925.00; ThrC 925.00; Th
10	dtRx_DQ_tMargin_DQS_DCD_Rj	DQSJS	<= 0.15 UI	-0.084 UI	Pass	A -0.00; B -0.03; C -0.01; D -0.08; ThrA 925.00; ThrB 925.00; ThrC 925.00; Th
11	tRx_DQS_DCD	DQSJS	<= 0.045 UI	0.045 UI	Pass	BER=1E-9; Conf=99.50; Conf_BER=1E-9; Patt=User111000; VClk=400.00; V
12	tRx_DQS_Rj	DQSJS	<= 0.0075 UI RMS	0.0075 UI RMS	Pass	BER=1E-9; Conf=99.50; Conf_BER=1E-9; Patt=User111000; VClk=400.00; V
13	tRx_DQS_DCD_Rj	DQSJS	<= 0.0525 UI	0.0525 UI	Pass	BER=1E-9; Conf=99.50; Conf_BER=1E-9; Patt=User111000; VClk=400.00; V
14	RxEW_at_BER_Stressed_Eye	STREYE	> 0 UI	0.297 UI	Pass	EwA=0.31; EwB=0.34; EwC=0.34; EwD=0.30; ThrA=914.00; ThrB=914.00; Th
15	RxBER_at_Center_Stressed_Eye	STREYE	<= 1E-16 BER	3.31e-46 BER	Pass	BerA=2.2e-46; BerB=3.5e-55; BerC=5.1e-55; BerD=1.1e-45; Align=Center; Bl
16	RxEH_Stressed_Eye	STREYE	~ 70 mV	70.1 mV	Pass	Stress_Cal=test4; Ampl=269.90; SI=125.00; SJ=0.0001; RJ=0.0214
17	RxEW_Stressed_Eye	STREYE	~ 0.25 UI	0.242 UI	Pass	Stress_Cal=test4; Ampl=269.90; SI=125.00; SJ=0.0001; RJ=0.0214
18	Vswing_Stressed_Eye	STREYE	<= 600 mV	270 mV	Pass	Stress_Cal=test4; Ampl=269.90; SI=125.00; SJ=0.0001; RJ=0.0214
19	Sj_Stressed_Eye	STREYE	<=0.45 UI	0.0001 UI	Pass	Stress_Cal=test4; Ampl=269.90; SI=125.00; SJ=0.0001; RJ=0.0214
20	Rj_Stressed_Eye	STREYE	<= 0.04 UI RMS	0.0214 UI RMS	Pass	Stress_Cal=test4; Ampl=269.90; SI=125.00; SJ=0.0001; RJ=0.0214
21	Vnoise_Stressed_Eye	STREYE	<= 125 mV	125 mV	Pass	Stress_Cal=test4; Ampl=269.90; SI=125.00; SJ=0.0001; RJ=0.0214
22	DFE_Gain_Stressed_Eye	STREYE	= 0 dB	0 dB	Pass	DFE_Gain=0dB
23	DFE_Taps_Stressed_Eye	STREYE	<= 60 sum |mV|	35 sum |mV|	Pass	Taps=-20, -5, -5, -5

Scale of the Problem

64 DQ LANES, 16 DQS LANES, 14 CA LANES AND REFCLK – 95 LANES PER MODULE

- Keeping track of results and test configurations when testing 95 lanes on multiple devices is an enormous task
  - This drives the need for a professional-grade database (SQL) of all results…

Summary of Key Challenges for Rx Testing

TOP FIVE

- Accurate stress calibrations so results can be compared from location to location, module to module
  - Accurate S-parameter models (measured, simulated, estimated) for all segments
- Selection of measurement depths, oscilloscope record sizes to make fast and accurate measurements
- Need for both conformance and “deep-dive” tests on DQ, CA and DQS, RefClk for DRAMS, DBs and RCDs
- Automating & Managing massive amounts of measurements and results
- Easy setup of a complex problem (with defaults) to get started but supporting intricate per-lane calibrations for later-on.

… all with a comfortable interface for Tx tests too

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Tektronix